ACSP · Analog Circuits And Signal Processing

Bupesh Pandita

Oversampling A/D Converters with Improved Signal Transfer Functions

Springer

Oversampling A/D Converters with Improved Signal Transfer Functions

ANALOG CIRCUITS AND SIGNAL PROCESSING SERIES

Consulting Editor*: Mohammed Ismail. *Ohio State University

For further volumes:
http://www.springer.com/series/7381

Bupesh Pandita

Oversampling A/D Converters with Improved Signal Transfer Functions

Springer

Bupesh Pandita
AMD
Markham, ON, Canada
bupesh.pandita@amd.com

ISBN 978-1-4614-0274-9 e-ISBN 978-1-4614-0275-6
DOI 10.1007/978-1-4614-0275-6
Springer New York Dordrecht Heidelberg London

Library of Congress Control Number: 2011934486

Abstract

This book proposes a low-IF receiver architecture suitable for the realization of single-chip receivers. To alleviate the image-rejection requirements of the front-end filters an oversampling complex discrete-time $\Delta\Sigma$ ADC with a signal-transfer function that achieves a significant filtering of interfering signals is proposed. A filtering ADC reduces the complexity of the receiver by minimizing the requirements of analog filters in the IF digitization path. Discrete-time $\Delta\Sigma$ ADCs have precise resonant frequency and clock frequency ratios and, hence, do not require the calibration or tuning that is necessary in the case of continuous-time $\Delta\Sigma$ modulator implementations. This feature makes the proposed discrete-time $\Delta\Sigma$ ADC ideal for multistandard receiver applications.

The $\Delta\Sigma$ modulator signal-transfer function (STF) and noise-transfer function (NTF) have been designed using complex filter routines based on classical filter design procedures. With a filtering STF and stop band attenuation greater than 30 dB, the $\Delta\Sigma$ modulator reduces intermodulation of the desired signal and the interfering signals at the input of the quantizer, and also avoids feedback of the high-frequency interfering signals at the input of the modulator.

The reported complex $\Delta\Sigma$ ADC is intended for DTV receiver applications. With a maximum intended sampling frequency of 128 MHz and an OSR of 16, the ADC has been designed to support a maximum DTV signal bandwidth of 8 MHz. Except for a somewhat reduced maximum sampling frequency, the test results of the prototype complex $\Delta\Sigma$ modulator are very close to the simulated results. The IC achieved 70.9 dB SNDR over a 6 MHz band centered around 3 MHz. The image rejection ratio (IRR) of the $\Delta\Sigma$ ADC was measured to be greater than 65 dB. The measurement results confirm the filtering characteristics of the ADC. The fabricated chip consumes 177 mW and occupies a silicon area of 2.15 mm^2.

Contents

List of Figures

List of Tables

Chapter 1
Introduction

1.1 Motivation and Background

Many applications require receiver designs that are small and low power, and have a small bill-of-material for passive components. These designs should also provide inexpensive, reliable, and easily manufactured receiver systems. These requirements call for integration of RF front-end and baseband processing in a single chip. Though the desirable case of converting directly from analog to digital at the antenna input does not seem to be feasible as yet, the trend is to include analog RF front-end with digital signal processing on the same chip.

Heterodyne architectures, due to their high performance and ease of implementation, continue to be employed in most modern receivers [1–6]. In these architectures, the input RF signal is down converted to an intermediate frequency (IF), amplified, and filtered before it is finally demodulated by a low-frequency demodulator. This demodulator is typically built to operate at frequencies below 100MHz; therefore, two intermediate conversions, with one IF sufficiently different from the RF signal, are often needed to facilitate image filtering. The multiple stages of IF filtering and amplification add to the complexity and cost of the receiver. Passive bandpass filters that offer high selectivity with high linearity and low noise, such as surface acoustic wave (SAW) filters, typically are used in the RF and IF stages to attenuate the interferers accompanying the desired signal. By attenuating interferer power prior to amplification, these filters greatly reduce the linearity and dynamic range requirements of the analog-to-digital converter (ADC) block used in the IF digitization. However, such filters are not amenable to on-chip implementation using present VLSI technology, and they limit the extent to which a receiver can be miniaturized.

An alternative is the direct conversion receiver (DCR), which promises superior performance in power consumption and size. This architecture has been seen as a potential solution for single-chip receiver implementations [7–8]. A power-splitter divides the RF input signal into two paths, which are further down converted by a quadrature mixer to in-phase (I) and quadrature (Q) baseband signals. Analog-to-digital conversion of each channel is performed at baseband

B. Pandita, *Oversampling A/D Converters with Improved Signal Transfer Functions*,
Analog Circuits and Signal Processing, DOI 10.1007/978-1-4614-0275-6_1,

frequency by a dedicated ADC, and the digital bits are processed by a digital signal processor (DSP). By down-converting the entire receive band directly to a baseband centered at or near dc (zero-IF or low-IF), usually less than 5MHz, the direct-conversion receivers allow most of the necessary amplification and interferer filtering to be performed by lowpass baseband amplifiers and filters, which are amenable to on-chip implementation. However, in contrast to superheterodyne receivers, the baseband components in a DCR must be highly linear, since they must pass the desired signal and at the same time reject the relatively large interfering signals; for example, in the case of a DVB-T (Digital Video Broadcasting - Terrestrial) receiver the interfering signal can be 45dB more powerful than the desired signal. Any interferer subjected to an even-order nonlinearity introduces a distortion product, which can potentially corrupt the dc or near-dc down-converted desired signal. In zero-IF DCRs, two additional problems are caused by the local oscillator having the same frequency as the RF desired signal: one, the local oscillator signal can inadvertently be radiated and interfere with other nearby receivers, and, second, the signal can couple to the RF mixer input port, and become down-converted to dc, and thereby contribute to a large unwanted offset on the down-converted desired signal. Circuit mismatches also contribute to dc offset, and flicker noise introduced by the baseband components directly corrupts the down converted desired signal.

Low-IF direct conversion receivers avoid the dc offset problems and are less sensitive to flicker noise, but are sensitive to gain and phase mismatches in their quadrature paths. These mismatches can cause interferers at image frequencies to corrupt the down-converted desired signal.

One of the important and growing trends in VLSI system integration is the shift of signal processing from the analog to the digital domain. In communication systems, this shift implies that the ADC is moved toward the front-end of the system, for example the antenna in the case of terrestrial reception. This usually increases the stringency of the ADC performance requirements, such as dynamic range and bandwidth. A signal seen at the front-end of a receiver typically consists of a desired signal centered at a frequency of interest and numerous interfering signals centered at surrounding frequencies. Thus, the receiver must have sufficient linearity that intermodulation products and aliased harmonics of the interferers do not impact the reference bit-error rate (BER). The fact that, at lower frequencies, analog circuits such as operational-amplifiers have higher gains and higher linearity justifies reducing the frequency of the IF signal and performing analog-to-digital conversion at a lower IF. The main advantage of using low-IF or zero-IF is that the required ADC bandwidth is as low as possible; however, in addition to downconversion of the desired signal to the IF, the frequency conversion is related to the conversion of the image frequency to the IF. This conversion of the image frequency to IF is known as the “image-band” problem [9].

Most existing receivers rely on analog filtering for rejecting interfering signals and use analog automatic gain control (AGC) to compensate for the wide dynamic

range of the desired signal. The result is that a precise analog-to-digital conversion is not usually necessary, and the conversion rate can be as low as the symbol rate of the transmitted signal. In integrated receivers, because of the reduction in power consumption and circuit complexity that can be achieved by trading analog processing for digital processing, the trend is to perform as much of the signal processing, for example, channel selection, in the digital domain. An advantage of this architecture is that the I/Q matching accuracy is very good, depending basically on the matching of the ADC input stage. The filters, as they are implemented digitally, can also have a very accurate frequency response and linear phase characteristic, that are important for digital modulation techniques. However, this interchange of channel filtering and ADC greatly increases the dynamic range and sample-rate required of the ADCs. ADCs with a resolution of more than 13-bits are typically required. This high-resolution requirement, together with wide Nyquist bandwidth (on the order of MHz), which is necessitated by high data-rate and to avoid aliasing of the interferes onto the down converted signal, necessitates the use of high performance ADCs. Among the wide variety of high-resolution ADC architectures, $\Delta\Sigma$ ADCs, with their high tolerance for component mismatches and lower power dissipation, are becoming increasingly popular in wireless receiver applications. However, the presence of interferers puts a severe demand on the linearity requirements of the analog circuitry and also calls for high-order digital filters to attenuate these interfering signals. For example, in Chap. 3 it has been demonstrated through behavioral model simulations that DAC nonlinearity in a $\Delta\Sigma$ modulator ADC cause aliasing of interfering signals into the signal band and result into a severe degradation of the ADC performance. Therefore, in such applications, it may be more desirable to have a filtering Signal Transfer Function (STF) with significant out-of-band attenuation instead of $\Delta\Sigma$ ADC with unity STF. Depending upon the application, e.g., single sideband (SSB), it may also be desirable to have higher attenuation in image band frequencies.

However, the design of an STF with higher stop-band attenuation has an implication for the quality of the Noise Transfer Function (NTF), and there is a trade-off involved in STF-NTF design. An independent STF and NTF design disregards the inherent STF-NTF trade-off and implements either an STF with reduced stopband attenuation or an NTF with degraded signal-to-noise ratio (SNR). The primary goal of this book is to develop an STF-NTF design methodology. The main challenges facing the design of a high SNR NTF and STF with significant out-of-band filtering are identified, and appropriate methodolgy to overcome these challenges is proposed. The impact of mismatches on a low-IF complex modulator is thoroughly investigated. A low-IF complex $\Delta\Sigma$ ADC modulator suitable for digital TV (DTV) receivers is developed. The specifications and requirements of an ADC suitable for digitization of DTV signals are studied, and both the system-level and the circuit-level requirements are derived. The analog circuitry required for the proposed complex modulator is implemented on a 0.18 μm CMOS chip. Extensive behavioral and circuit simulations and measurements of the test-chip result verify the proposed NTF-STF co-design methodology.

1.2 Digital TV (DTV) Receivers

Figure 1.1 [10] shows a functional block diagram of a DTV receiver. The functional blocks of a modern DTV receiver are:

- Tuner, including RF amplifiers, automatic gain control (AGC), filtering, and the local oscillator (LO) and mixer (or pair of LOs and mixers in the case of double conversion tuners) needed to down-convert the desired RF channel frequency to that of the intermediate frequency (IF).
- IF filter and amplifier, which condition the signal to exploit the full ADC dynamic range. This block usually includes major portion of the predecoding gain, channel selectivity, and some desired-channel band-shaping.
- ADC
- Digital demodulator, which includes in-band interference rejection, multipath cancellation, and signal recovery.

In addition, the digital receiver may include other blocks, e.g., Forward Error Correction (FEC) for detecting and correcting errors in the demodulated digital stream or synchronization blocks to detect carrier and phase offsets.

The frequency of the DTV receivers covers the range between 42 and 1000 MHz. There are two different architectures of the DTV receiver chip that have been in common use in the industry: (1) single-conversion; see Fig. 1.2, and (2) double-conversion; see Fig. 1.3.

The single-conversion architecture directly down-converts the RF signal to an IF (about 44 MHz). The single-conversion receivers rely on front-end "tracking filters" for image suppression. Often, these filters are divided in to Low VHF, high VHF, and UHF bands to cover the whole frequency range. The single-conversion architecture, which traditionally is implemented with Bipolar or Bi-CMOS processes, has been widely used in DTV tuner ICs [4,9].

The double-conversion DTV receiver architecture up-converts the RF signal to an IF, which is higher than the highest frequency in the input frequency range (about 1.2 GHz), and then, using a fixed frequency mixer, down-converts the IF to a second IF (about 36 – 44 MHz). Though, dual-conversion architecture can realize high image-rejection, it suffers from high power consumption. In addition two

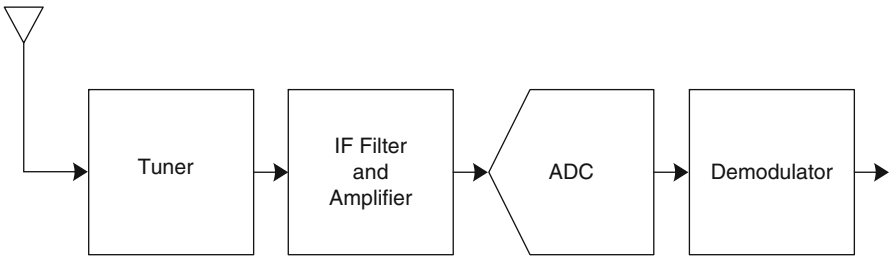


Fig. 1.1 DTV receiver front-end block diagram

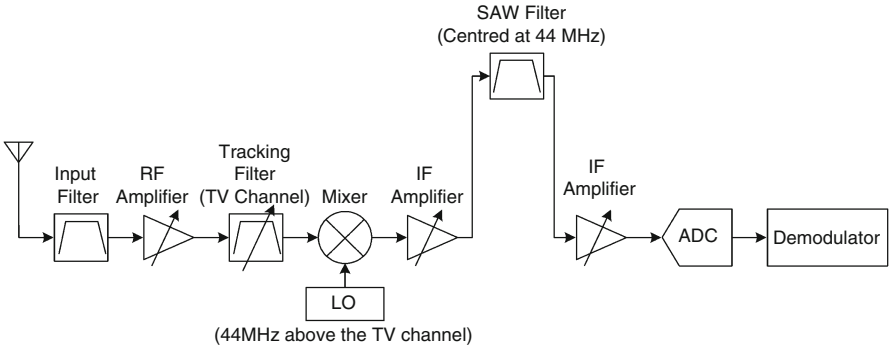


Fig. 1.2 Single-conversion DTV receiver block diagram example

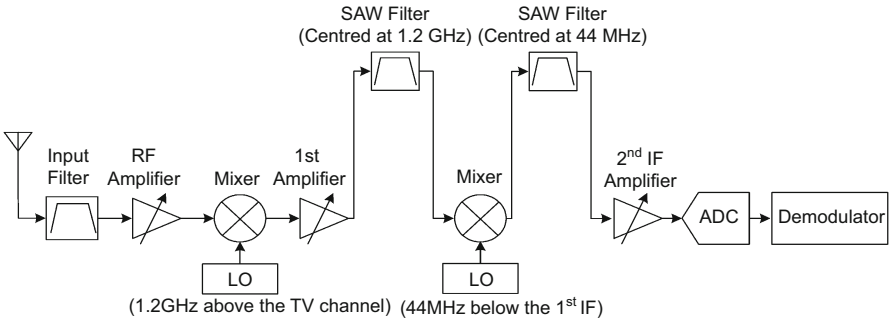


Fig. 1.3 Double-conversion DTV receiver block diagram example

off-chip SAW filters are usually required for signal selection and image rejection, and these external filters limit the integration level and add to the cost of the receiver.

A direct-conversion receiver architecture for the European digital video broadcasting for hand-held (DVB-H) has been proposed in [7]. An off-chip band-limit filter at the input is used to suppress the undesired signals, and an external LNA has been employed to satisfy the noise requirement. The IC uses on-chip eighth order, inverse Chebyshev low-pass filtering for channel selectivity, and RF tunable bandpass filter and a polyphase mixer for harmonic rejection. The I/Q mismatch errors have been addressed by the digital signal processing (DSP) in the demodulator, but frequency-dependent errors have been minimized by circuit design and layout. The IC has integrated a DC-offset correction system. Image rejection and channel filtering have been implemented digitally. The receiver is implemented in a 0.35 μm SiGe BiCMOS technology and consumes 240 mW from a 2.775 V supply.

A dual-conversion multi-standard analog and digital TV architecture has been reported in [5]. The receiver consists of an up-conversion mixer, a digitally gain-programmable image reject down-conversion mixer, and relies on two external first- and second-IF SAW filters for channel filtering. The receiver is implemented

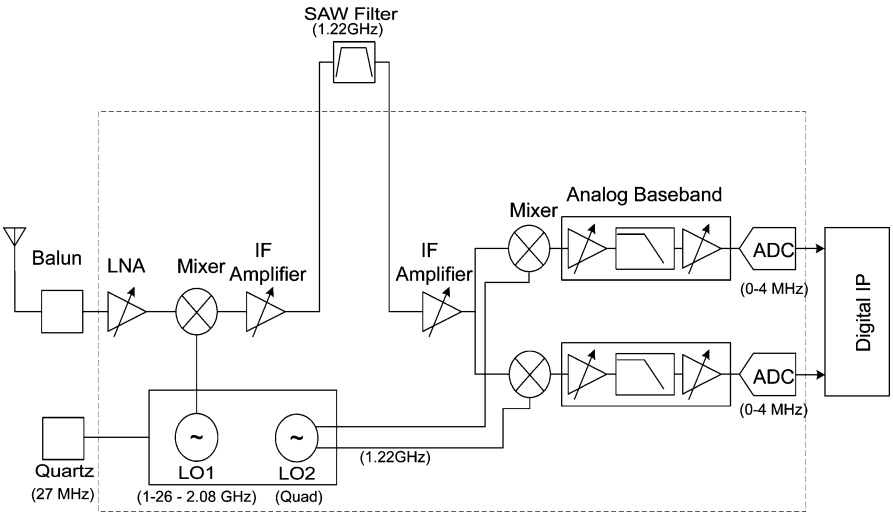


Fig. 1.4 Double-conversion DTV receiver block diagram [2]

in a 0.35 mm SiGe BiCMOS technology and consumes 1.5 W from a split 5 V and 3.3 V supply.

Besides the single- and double-conversion architectures, other architectures have been reported in the literature. A double conversion zero second-IF (DZIF) DVB-T receiver chip has been reported in [2]; refer Fig. 1.4. In this architecture, the desired RF signal is first up-converted to an intermediate frequency of 1.22 GHz and then quadrature down-converted to a zero intermediate frequency. Channel filtering is partially performed by an external SAW filter centered at the first intermediate frequency. The I and Q outputs of the quadrature mixer are digitized by two 14bits 4 MHz bandwidth $\Delta\Sigma$ ADC modulators. The IQ gain mismatch is corrected in the analog domain, and the phase mismatch is corrected by digital algorithms processing the ADC outputs. The receiver has been implemented in a 2.5 V, 0.12 μm CMOS technology and consumes 1.4 W.

A double-conversion, low-IF, multi-standard TV receiver chip has been reported in [6]. The proposed receiver uses an up-conversion followed by a quadrature down-conversion mixer to shift the desired channel to a frequency of 1.75 MHz. The complex outputs of the quadrature mixer are filtered with a complex low-pass filter and finally digitized by two 11bit ADCs. The chip does not use any external SAW filters, and channel filtering and in-band image rejection are performed in the digital domain. The receiver, which is fabricated in a 0.25 μm CMOS technology, consumes 1W from a 2.5 V supply.

Over the past few years, there has been a marked shift from high-IF dual-conversion to low-IF single-conversion architectures. A single-conversion, low-IF receiver architecture for multi-standard TV has been presented in [8] [Fig. 1.5]. Quadrature mixing is used to down-convert the desired channel to a low intermediate frequency (4.57 MHz). The architecture splits the quadrature mixer into three

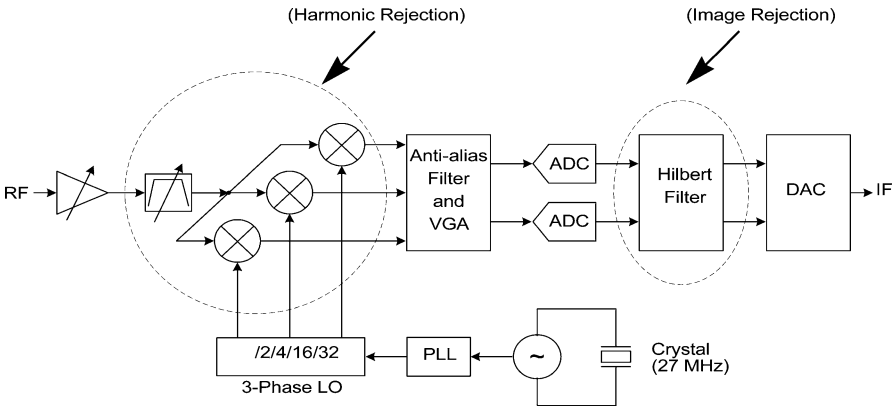


Fig. 1.5 Single-conversion DTV receiver architecture [8]

individual mixers. A coarse, selectable filter, together with the three-phase mixers, is used for harmonic rejection. Two 11b pipelined ADCs are used for the digitization of the I and Q signals. The image rejection has been performed digitally. The chip which is implemented in a 0.18μm CMOS process, consumes 750 mW from a single 1.8 V supply.

1.3 Outline

This book is organized as follows: In Chap. 2, a low-IF complex ΔΣ modulator-based DTV receiver is presented. The chapter provides background information on real and complex mixing and on how complex-mixing is ideally suited for on-chip integration. A low-IF receiver architecture that alleviates some of the problems faced by a zero-IF receiver is presented. A major problem faced by receivers handling wireless signals is the presence of interfering signals or "interferers", which are usually stronger than the desired signal, and accompany the desired signal. Often, intermodulation products generated by these interferers and the desired signal limit the SNR of the receiver. After a discussion of the "interfering signals" problem in DTV receivers, the chapter presents and compares the existing approaches used to filter interfering signals in ΔΣ modulator ADC-based receivers. Finally, the chapter concludes by deriving specifications for a low-IF complex ΔΣ modulator ADC suitable for a DTV receiver.

Chapter 3 starts with background information on the norm and how it can be used in the design of an NTF. The chapter discusses the trade-off involved in the design of an NTF and an STF; further, the need for developing an NTF-STF co-design methodology is explained. The chapter presents design methodology for deriving NTFs, and STFs (real and complex) with significant stop-band

attenuations. Finally, the advantages of the proposed ΔΣ ADC modulator with filtering STF are presented.

In Chap. 4, architecture-level design and simulations of the proposed ΔΣ modulator are presented. The impact of circuit mismatches on a complex ΔΣ ADC modulator and the need for stage-ordering are presented. The complete fourth order ΔΣ ADC modulator architecture is presented in this chapter. The transition from the Simulink™ [12] model to the switched-capacitor (SC) circuit is presented. There is consideration of the impact of SC circuit non-idealities, e.g., the settling errors of the integrators, finite gain of the Opamp, finite resistance of the sampling switches, random jitter in the sampling clock, capacitor mismatches, and multi-level DAC nonlinearity, on the SC circuit specifications.

Chapter 5 presents the circuit-level design and simulation of the blocks proposed in Chap. 4. The circuit of the SC ΔΣ ADC modulator consists mainly of opamp, multi-bit quantizer, multi-level DAC, non-overlapping clock generators, switches, and biasing. A detailed description of the design of the various blocks in the SC ΔΣ ADC modulator is presented. Finally, the layout techniques for capacitors, switches, quantizers, Opamp and the complete fourth order modulator are presented. Further, the chapter describes the experimental testing of the fabricated chip. The test set-up, including the fabricated chip, and the designed printed circuit board (PCB), is presented in the chapter. The measured results are also reported.

Chapter 6 concludes the book and suggests directions for future research.

References

1. Mehr, I.: Integrated TV tuner design for multi-standard terrestrial reception. In: IEEE Radio Frequency Integrated Circuits Symposium, pp. 75–78, 12–14 June 2005
2. Saias, D., Montaudon, F., Andre, E., Bailleui, F., Bely, M., Busson, P., Dedieu, S., Dezzani, A., Moutard, A., Provins, G., Rouat, E., Roux, J., Wagner, G., Paillardet, F.: A 0.12um CMOS DVB-T tuner. IEEE International Digest of Technical Papers. ISSCC, pp. 430–431, 2005
3. Dawkins, D., Burdett, A.P., Cowley, N.: A single-chip tuner for DCB-T. IEEE J. Solid-State Circuits. **38**(8), 1307–1317 (2003)
4. van Rumpt, H., Kasperkovitz, D., van der Tang, J., Nauta, B.: UMTV: a single chip TV receiver for PDAs, PCs, and cell phones. In: IEEE International Digest of Technical Papers. ISSCC, pp. 428–429, February 2005
5. Stevenson, J.-M., Hisayasu, P., Deiss, A., Abesingha, B., Beumer, K., Esquivel, J.: A multi-standard analog and digital TV tuner for cable and terrestrial applications. In: IEEE International Digest of Technical Papers. ISSCC, pp. 210–213, February 2007
6. Heng, C.-H., Gupta, M., Lee, S.-H., Kang, D., Song, B.-S.: A CMOS TV tuner/demodulator IC with digital image rejection. In: IEEE International Digest of Technical Papers. ISSCC, pp. 432–433, February 2005
7. Antoine, P., Bauser, P., Beaulaton, H., Buchholz, M., Carey, D., Cassagnes, T., Chan, T.K., Colominers, S., Hurley, F., Jobling, D., Kearney, N., Murphy, A., Rock, J., Salle, D., Tu, C.-T.: A direct-conversion receiver for DVB-H. In: IEEE International Digest of Technical Paperss. ISSCC, pp. 426–427, February 2005
8. Gupta, M., Lerstaveesin, S., Kang, D., Song, B.-S.: A 48-to-860 MHz direct-conversion TV tuner. In: IEEE International Digest of Technical Papers. ISSCC, pp. 206–208, February 2007

9. Mirabbasi, S., Martin, K.: Classical and modern receiver architectures. IEEE Commun. Mag. **38**(11), 132–139 (2000)
10. Henderson, J.G.N., Bretl, W.E., Deiss, M.S., Goldberg, M.S., Markwalter, B., Muterspaugh, M., Touzni, A.: ATSC DTV receiver implementation. Proceedings of the IEEE, vol. 94, No. 1, pp. 119–147, January 2006
11. TUA 9001, RF Silicon Tuner for DVB-H/T and CMMB (Direct Conversion Recever), INFINEON Technologies.
12. The Math Works, Inc., Matlab, Version R2007a, Natick, Massachusetts: The Math Works, Inc., 2007

Chapter 2
A Low-IF Complex ΔΣ ADC-Based DTV Receiver

This chapter provides background information regarding the "image-band problem" that is related to frequency conversion, complex filters, mismatch issues associated with complex filters, and "interfering-signals problem" in wireless receivers.

As the analog television broadcast system is being phased out and replaced by all-digital transmission in recent years, research has been conducted to develop digital television (DTV) receivers. However, for the available DTV receiver solutions, the issues of low-power and low-cost design still remain there. For example, most commercial DTV receivers use a dual-conversion architecture and are implemented with expensive technologies like SiGe and BiCMOS, instead of with low-cost CMOS technology. These receivers rely on external surface-acoustic wave (SAW) filters for image rejection and channel selection. This chapter presents a low-IF complex ΔΣ modulator-based receiver architecture suitable for realization of a highly integrated DTV receiver with CMOS technology.

Signals seen at the front-end of a wireless receiver typically consist of a desired signal accompanied by strong interfering signals. Though ΔΣ ADCs with wide dynamic range are suitable for digitizing such signals, there is often a need to pre-filter these signals due to the linearity and power requirements of the analog circuits. This chapter reviews some of the solutions for handling the interfering signals in ΔΣ modulator-based wireless receivers and presents their advantages and disadvantages. The benefits of ΔΣ ADC with integral filtering for digitizing signals accompanied by high interfering signals are outlined. In the next chapter, a design methodology for the realization of a ΔΣ modulator with a filtering signal transfer function (STF) is presented.

B. Pandita, *Oversampling A/D Converters with Improved Signal Transfer Functions*, Analog Circuits and Signal Processing, DOI 10.1007/978-1-4614-0275-6_2,

2.1 Background

2.1.1 Bandpass Signals

Fig. 2.1 shows spectrum of a real-valued signal, with spectrum centered at a non-zero frequency, f_c. The bandpass signal could be represented as:

$$x(t) = x_1(t)\cos(2\pi f_c t) - x_Q(t)\sin(2\pi f_c t) \tag{2.1}$$

The components, $x_I(t)$ and $x_Q(t)$, can be viewed as real-valued lowpass signals impressed on the carrier frequency, f_c. $x_I(t)$ and $x_Q(t)$ are referred to as in-phase (I) and quadrature (Q) component of the bandpass signal.

Real-valued signals are characterized by spectrum with:

- amplitude symmetric around zero frequency (DC), and
- phase antisymmetric around zero frequency (DC).

$$X(f) = X^*(-f) \tag{2.2}$$

where $X(f)$ is the frequency spectrum of $x(t)$.

2.1.2 Complex Signals

Complex signals can be thought as a representation of a pair of real signals. For example, for a pair of wires at voltages V_1 and V_2, we may represent the pair of wires as carrying a "complex voltage" $V \equiv V_1 + jV_2$. Similarly, for a pair of time varying signals, $f_1(t)$ and $f_2(t)$, one can consider it as a complex signal, $f(t) \equiv f_1(t) + jf_2(t)$.

The complex signals differ from real signals in the frequency domain. For real signals the frequency spectrum must be symmetric about DC, however, no such constraint applies for the complex signals, and complex signals can be asymmetric about DC. Fig. 2.2 shows frequency spectrum of real signals $V_1 = \cos(2\pi f_c t)$, and complex signal $V = \cos(2\pi f_c t) + j\sin(2\pi f_c t)$. Compared to double impulses for

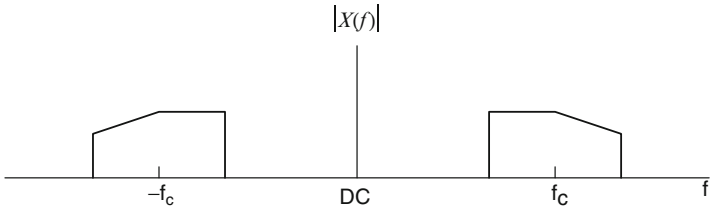
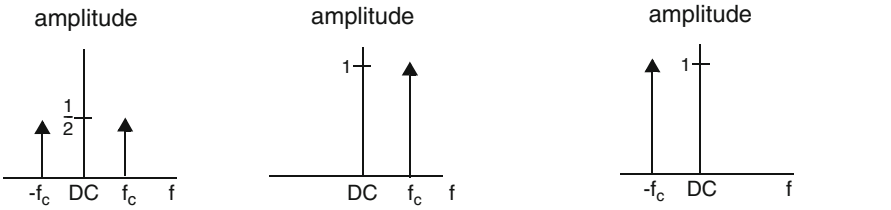


Fig. 2.1 Spectrum of a bandpass signal



$V_1 = \cos(2\pi f_c t)$ $V = \cos(2\pi f_c t) + j\sin(2\pi f_c t)$ $V^* = \cos(2\pi f_c t) + j\sin(2\pi f_c t)$

Fig. 2.2 Spectrum of real and complex signals

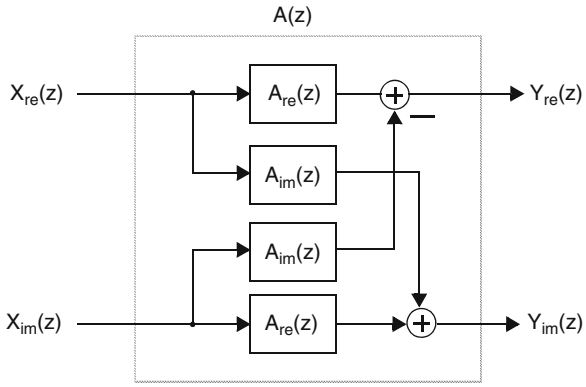


Fig. 2.3 Realizing a complex filter with real filter blocks

V_1 at frequencies f_c, V has power only at positive frequency f_c. A conjugate signal, V^*, with power only at negative frequency $-f_c$ is defined as image of signal V; for example, $V^* = \cos(2\pi f_c t) - j\sin(2\pi f_c t)$ is image of signal V.

2.1.3 Complex Filters

A *complex* filter has a transfer function with complex-valued coefficients [1]. Unlike a real filter, a complex filter is not constrained to have conjugate poles and zeros, and, as a consequence, is not restricted to a symmetrical magnitude response around DC. This can be useful in some situations, for example the use of polyphase filters to generate single sideband signals.

Though the input and output of a complex filter are complex, the filter is constructed from several cross-coupled *real* filters, as shown in Fig. 2.3.

If there is a complex input signal

$$X(z) = X_{re}(z) + jX_{im}(z) \tag{2.3}$$

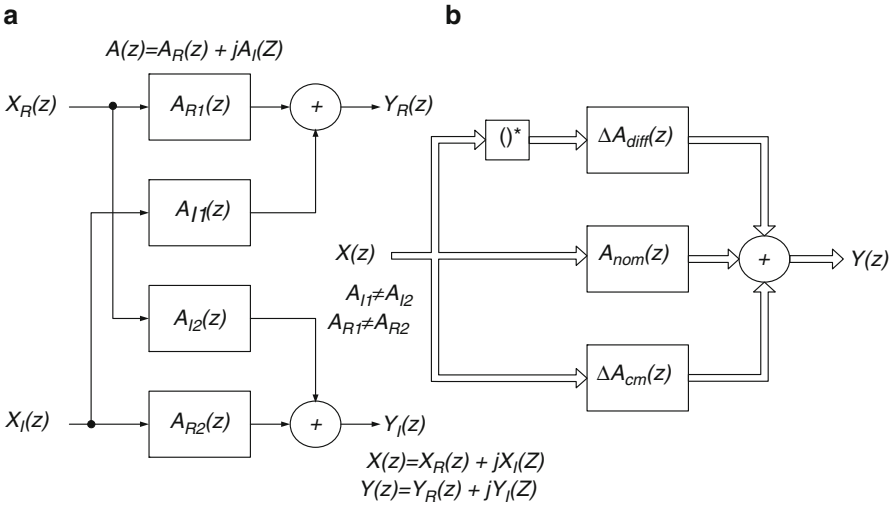


Fig. 2.4 (**a**) Complex filter constructed from non-ideal components, and (**b**) Signal flow diagram of a complex filter A(z), showing common-mode and differential error components

input to a complex transfer function

$$A(z) = A_{re}(z) + jA_{im}(z), \tag{2.4}$$

then the complex output signal is:

$$Y(z) = Y_{re}(z) + jY_{im}(z) = A(z)X(z) \tag{2.5}$$

$$Y(z) = [A_{re}(z)X_{re}(z) - X_{im}(z)\,A_{im}(z)] + j[A_{re}(z)X_{im}(z) + X_{re}(z)A_{im}(z)] \tag{2.6}$$

2.1.4 Mismatch in Complex Filters

In circuit realizations of a complex filter, due to component mismatches, etc., the two real-part transfer functions may not be equal, and the same variation may be true for the two instances of the imaginary-part transfer functions. In [2] and [3], it has been shown that the transfer function of the mismatched complex filter can be written as a nominal term, a common-mode error term, and a differential-error term; refer to Fig. 2.4.

The output of the filter can be written as

$$Y(z) = A_{nom}X(z) + \Delta A_{cm}X(z) + \Delta A_{diff}X^*(z) \tag{2.7}$$

where $X^*(z)$ denotes complex conjugate of $X(z)$, and the error transfer functions are defined as

$$\Delta A_{cm}(z) = \left\{\frac{A_{R1} + A_{R2}}{2} - A_{Rnom}(z)\right\} + j\left\{\frac{A_{I1} + A_{I2}}{2} - A_{Inom}(z)\right\} \tag{2.8}$$

$$\Delta A_{diff}(z) = \left\{\frac{A_{R1} - A_{R2}}{2}\right\} + j\left\{\frac{A_{I1} - A_{I2}}{2}\right\} \tag{2.9}$$

The term ΔA_{cm} represents a common-mode variation of A_{R1} and A_{R2}, and similarly ΔA_{diff} is the differential variation in A_{R1} and A_{R2}.

The effect of differential term, (2.9), is that it causes conjugation of the image-band and the desired signal-band. The undesired input signal band, which will be superimposed on the desired signal band after conjugation, is called the "image-band." This aliasing of image frequency into desired signal can seriously degrade the quality of the desired signal at the output. The aliasing or leakage of image frequency into signal-band is quantified by *image rejection* of the complex system. The aliasing of signal-band into image-band is usually not an issue. The common-mode variation, ΔA_{cm}, is usually small compared to A_{nom} and can be ignored.

2.1.5 Real Mixing vs. Complex Mixing

Continued on-chip integration of receiver front-ends has resulted in the lowering of the intermediate frequency (IF). The fact that at lower frequencies analog circuits like operational-amplifiers have higher gains, and higher linearity justifies frequency down conversion to a lower non-zero IF signal and performing analog-to-digital conversion at the lower IF. However, frequency conversion is related to "image-band" problem [4] as described in Sect. 2.1.4, which is actually downconversion of two frequency bands symmetric to the multiplying frequency to the same output band. Frequency down-conversion of a passband signal is typically performed by mixing the signal with a sinusoid, e.g., $\cos(2\pi f_{LO}t)$. This is shown pictorially in Fig. 2.5.

The spectrum of the mixer output signal is the superposition of the positive and negative shifted versions of the spectrum of the input signal. As is shown in Fig. 2.5, the two frequency bands that are symmetrical around the multiplying frequency are down-converted to the same output band. It is necessary to suppress any signal in the image band prior to the mixing operation. This is the task of the image-reject (IR) filter, which usually precedes the mixer. The previously discussed image problem arises due to the fact that the frequency spectrum of a real sinusoid contains impulses at both positive and negative frequencies. As shown in Fig. 2.6, one way to avoid this problem is to mix the signal with a complex exponential, e.g., $e^{-j2\pi f_{LO}t}$, which has only a single frequency component, in this

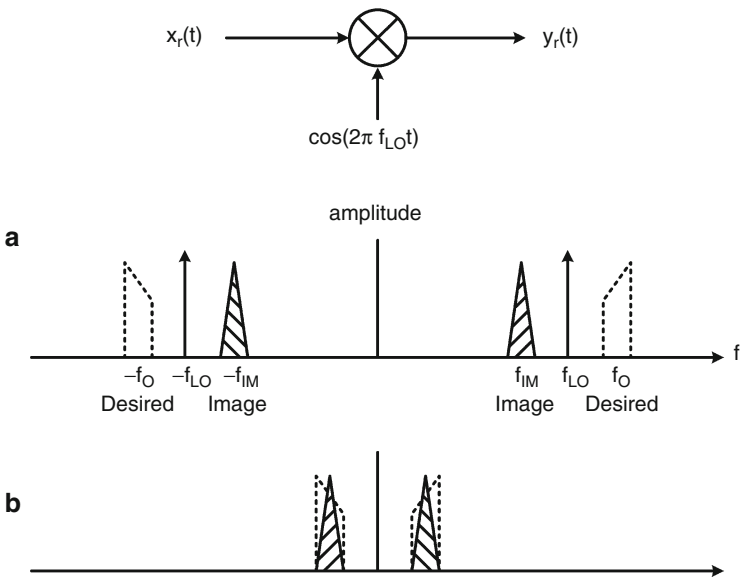


Fig. 2.5 Mixing a real signal with a sinusoid: **(a)** mixer input spectra, **(b)** mixer output spectrum

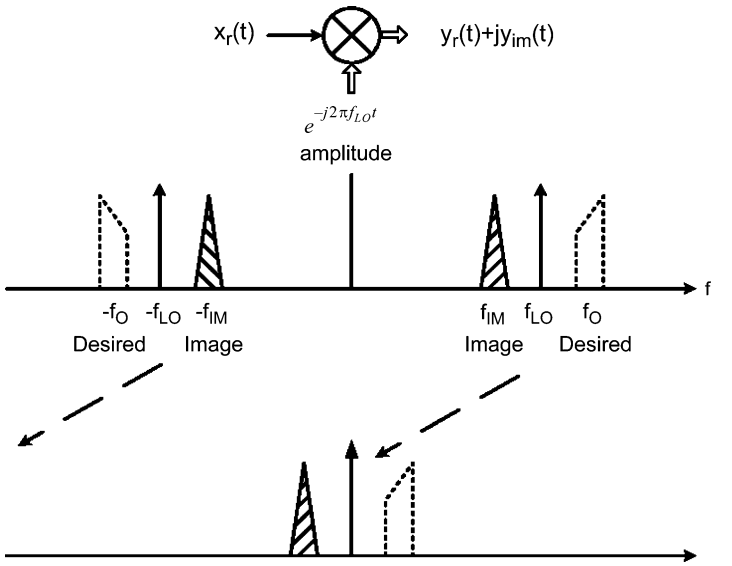


Fig. 2.6 Mixing a real signal with a complex exponential

case at a negative frequency, $-f_{LO}$. Therefore, mixing a real signal with this negative-frequency complex exponential results in a complex signal whose spectrum is a shifted version of the real signal spectrum. Theoretically, this process eliminates the image problem associated with frequency shifting when mixing is done with a real sinusoid. Although a quadrature signal path is needed for suppression of signals at the image frequency, this topology is still favorable due to performance and efficiency in terms of power consumption. Almost all modern receivers employ quadrature demodulation. The quadrature demodulation is performed by an I/Q mixer that uses two local oscillators with a same frequency, but a 90° phase difference. The I and Q components are independent and orthogonal to each other.

As discussed in Sect. 2.1.5 mismatches in the complex path cause undesired *image-frequencies* to alias into the desired signals. For a gain error of ΔG from the nominal gain of G and phase error of $\Delta\phi$ between the two paths of a quadrature system, "image rejection ratio" IRR is given by

$$IRR \approx \frac{\Delta\phi^2 + (\Delta G/G)^2}{4};\ (\Delta\phi \ll 1, (\Delta G)/G \ll 1) \tag{2.10}$$

For an IRR of 60 dB the gain and phase mismatches between the two paths of the quadrature system have to be less than 0.1% and 0.1˚, respectively. Often, the IRR is limited to less than 40 dB, and gain-phase calibration or additional filtering is required to improve IRR of the system [5].

2.1.6 Complex Transfer Function Design

A complex frequency response symmetric around a center frequency can be obtained by frequency shifting of a real response- the frequency shift in z-plane means rotation of the real response filter pole-zero constellation. Fig. 2.7a shows a pole-zero constellation of a lowpass filter with equiripple stopband response. In Fig. 2.7b the pole-zero constellation has been rotated by $\pi/4$ to realize the shifted complex magnitude response shown in Fig. 2.7d. What this example highlights is that all the standard methods for designing real filters can be applied in the realization of symmetric complex filters. A simple design procedure for obtaining the complex filter transfer using MATLAB involves following steps:

$$[z, p, k] = cheby2(4,\ 60,\ 1\ /\ 4)$$

The complex pole-zero constellation $(\hat{z}, \hat{p})$ shown in Fig. 2.7c has been realized from the real pole-zeros (z, p) by:

$$\hat{z} = z \times e^{i(\pi/4)}$$
$$\hat{p} = p \times e^{i(\pi/4)}$$

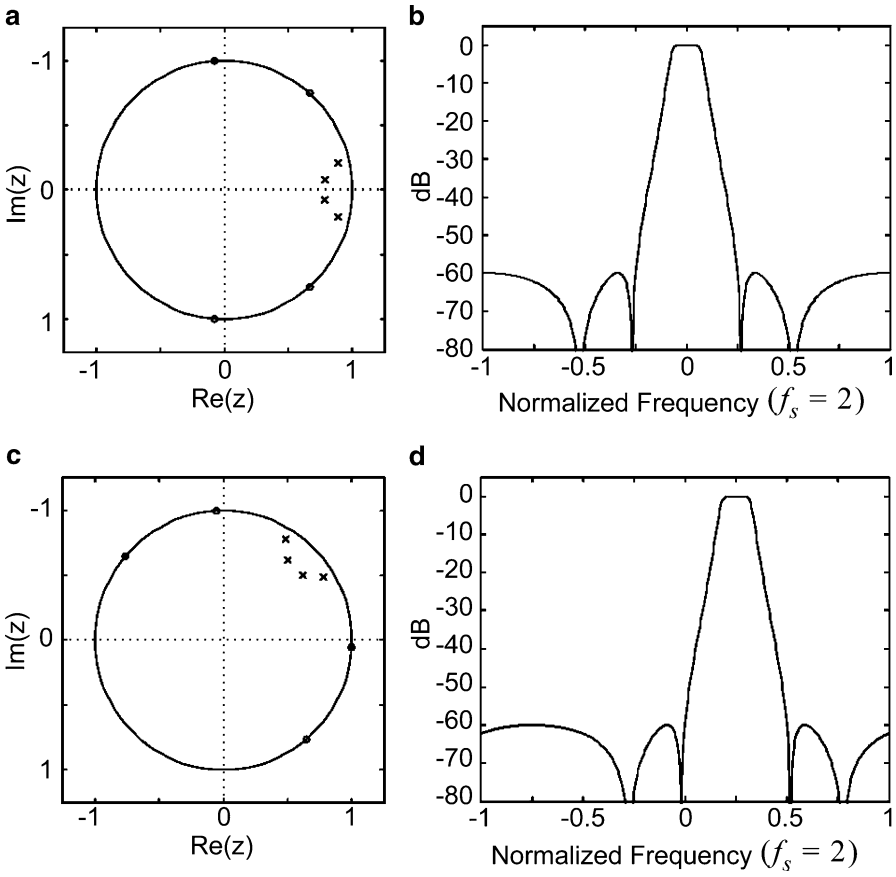


Fig. 2.7 Low pass filter methodology used to realize symmetric complex filter. Real lowpass filter: (**a**) Pole-zero constellation. (**b**) Magnitude Response. Complex bandpass filter designed by rotation of the lowpass pole-zeros: (**c**) Pole-zero constellation., (**d**) Magnitude Response

A methodology to design complex response bandpass transfer functions without the requirements of first designing a real response transfer function has been described in Chapter 3.

2.2 A Low-IF DTV Receiver Architecture

Fig. 2.8 presents a digital DTV receiver architecture built around a low-IF *complex* ΔΣ modulator [6]. In the proposed architecture, a single down-conversion step divides the input signal into quadrature branches at a low-IF frequency. The high-Q RF image reject filter in the traditional receiver architecture has been replaced by a

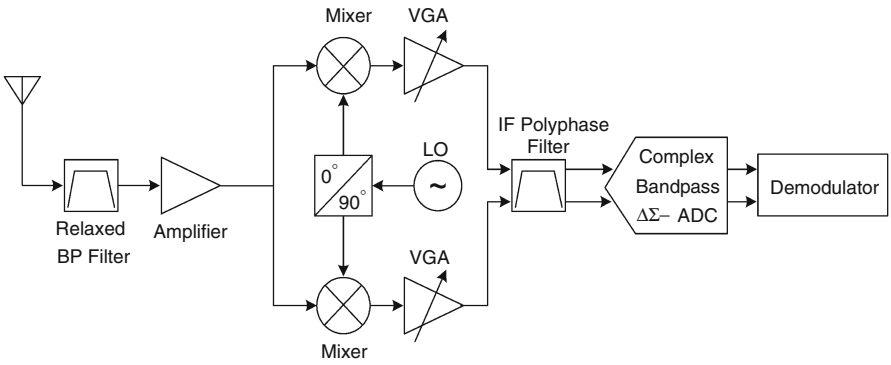


Fig. 2.8 A quadrature-IF system using a complex Low-If ΔΣ modulator

relaxed low-Q bandpass filter [7]. In the low-IF receiver, the IF has been modified to a low but non-zero frequency value; the frequency value falls into the baseband signal-processing capabilities of the analog circuits. An architecture based on low-IF eliminates some of the detrimental effects, e.g., DC-offset, LO self-mixing, second order intermodulation, that are faced by the direct-conversion scheme. The main drawback of the low-IF architecture is that the image band interference is close to the desired signal, and it is difficult to separate the image frequency from the desired signal through the use of relaxed low-Q bandpass filters. The mismatches between the in-phase (I) and quadrature (Q) channels cause an aliasing of the image frequency into the desired channel. Since the image frequency can be significantly stronger than the desired signal, the image rejection requirements of the receiving system may demand a higher matching of the in-phase (I) and quadrature (Q) channels.

The dual ADCs in the traditional low-IF receiver architecture have been replaced by a complex low-IF ΔΣ ADC. The low-IF has been selected at a value of 3 MHz for ATSC and 4 MHz for DVB-T standards. At a maximum sampling frequency of 128 MHz, and an over-sampling ratio (OSR) of 16, the architecture is suitable for digitization of the maximum DTV signal bandwidth of 8 MHz. The two anti-alias filters in the traditional dual ADC architecture have been replaced by a single complex bandpass anti-aliasing filter, and the replacement is advantageous since the same complex bandpass filter can be designed for alias rejection and also for image signals rejection. A low-IF means lower Q bandpass poles, practical resistor and capacitor ratios, and a low sensitivity of the bandpass filter center frequency to the errors in the RC time constants.

Among the wide variety of high-resolution ADC architectures, ΔΣ ADCs, with their reduced sensitivity to component mismatches and lower power dissipation, are becoming increasingly popular in systems that have stringent performance requirements such as wide dynamic range, wide bandwidth, and low power. The presence of interferers puts a severe demand on the linearity requirements of the analog circuitry in a wireless receiver, and often the intermodulation products generated due to the non-linearities of the receiver limit the system's signal-to-noise

ratio (SNR). An advantage of ΔΣ ADCs over other ADC architectures is that for a given dynamic range over a narrow passband and sufficient linearity to accommodate interferers over a large frequency band, ΔΣ ADCs tend to consume less power than other ADC architectures that have comparable linearity but achieve the full dynamic range over a larger frequency band [8]. With a large dynamic range and high linearity, ΔΣ ADCs allow for reduced analog baseband components and transfer much of the baseband filtering from the analog to the digital domain.

In a receiver system based on dual "one-input and one-output" ΔΣ modulators, the same ΔΣ modulator performs analog-to-digital conversion on not only the signal component but also on an image component. In contrast, a complex ΔΣ modulator, with no constraints of poles and zeros to be in conjugate pairs, digitizes only the signal component. For a given OSR and sampling rate, the complex ΔΣ ADC signal bandwidth is effectively halved and this halving translates into almost double the power efficiency as compared with a dual ΔΣ ADC approach. Further, with a multi-bit complex quantizer and a multi-level digital-to-analog converter (DAC), the requirements for performance of the internal operational amplifiers are moderate, and a larger SNR can be implemented by a low-order loop filter. The main advantages of a complex low-IF architecture are that offset and also flicker noise do not interfere with the desired signal; self-EMI is not an issue because the local-oscillator frequency is different from the carrier frequency. As in any bandpass system, only odd-order distortion products have an effect. A complex-IF mixer alleviates the image problem, so that the front-end filter can have relaxed specifications and thus reduced size.

DSP algorithms at the digital backend can be employed to compensate for I/Q imbalance, complex down-conversion, equalization, etc. Furthermore, signal processing, like channel selection, demodulation are performed in the digital domain, and this feature gives the architecture the advantages of flexibility with respect to multi-standards.

2.3 The 'Interfering Signals' Problem in Wireless Receivers

A typical RF signal received at the input of a wireless receiver consists of a desired signal along with numerous interfering signals, which are usually stronger than the desired signal. The ATSC Receiver Performance Guidelines [9] describe the minimum desired-to-undesired (D/U) channel ratio, under which the DTV receivers should exceed the reference bit-error-rate (BER).[1] For example, according to [9], there can be an interferer six channels (36 MHz) away that has 57 dB higher power than the desired channel.

[1] At this BER level, the error protection can correct most of the data errors and deliver a high quality picture.

Similarly, DVB-T/H receiver standards [10] define signal reception conditions in the presence of other interfering digital and analog TV channels. DVB-T [10] defines two different interference pattern sets that may be used to test the immunity of the DTV receiver to interferences. The first set, which tests the selectivity of the receivers, includes two separate interferer patterns, i.e., S1 and S2:

- S1 pattern: analog interference signals from PAL/SECAM TV (S1 pattern), especially PALG interference, defined as 35 dB stronger than the wanted 64-QAM signal. The carrier of the analog TV signal is located a single channel away from the center of the wanted signal;
- S2 pattern: a digital TV channel two channels away and up to 40 dB stronger than the wanted signal.

For a low-IF receiver architecture, these requirements translate into sharp channel select filters and high linearity of the receiver.

The second set tests the non-linearity of the receiver with three different interferer patterns: L1, L2, and L3, each consisting of two interferers:

- one digital interferer and one analog interferer, two and four channels away from the wanted channel. The interfering channels can be 40 dB and 45 dB stronger than the wanted signal;
- two analog interferers, two and four channels away from the wanted channel. The interfering channels can be 45 dB stronger than the wanted signal;
- two digital interferers, two and four channels away from the wanted channel. The interfering channels can be 40 dB stronger than the wanted signal.

The presence of other interfering signals, e.g., GSM interference from cell-phone up-link, add to the linearity and filtering requirements of the receiver.

In addition, the receiver's non-linearity can also generate interferences to DTV reception. The inter-modulation among the interfering channels or cross-modulation between the interfering channels and the desired channel creates distortion or noise components that fall in the desired channel. For example, interference from undesired signals on channels in the form N+K and N+2K (N is the desired channel) can cause two third-order intermodulation products falling in the channels N and N+3K [11]. Narrow tracking filters for rejecting these interfering signals are not amenable to silicon integration, and, as a result there is a large frequency range of signals present at the input of an analog-to-digital converter in a receiver. The receiver has to reject these interfering signals and detect the transmitted bit sequence. The presence of interfering signals requires that the analog-to-digital converters, in addition to handling large signal dynamic range and bandwidth, must have sufficient linearity that intermodulation products and aliased harmonics of the interferers do not impact the reference BER.

2.4 Approaches to Filtering Interfering Signals in ΔΣ ADC Based Receivers

The interfering signals accompanying a desired signal may be filtered by digital filters processing the ADC output, or they may be suppressed by an analog filter at the input of the ADC. An alternative topology includes filtering as an integral part of the ADC.

2.4.1 Filtering Interfering Signals in the Digital Domain

The first solution to handling interferers consists of using an analog-to-digital converter, typically a ΔΣ ADC, with a relaxed broadband analog filter at the front-end. Due to its inherently anti-aliasing nature, in a continuous-time ΔΣ ADC, an anti-aliasing analog filter of a lower order may be sufficient to meet the alias suppression requirements of the ADC. The analog signals at the input of the ADC comprise the desired signals and possibly the adjacent channel's interfering signals. The presence of interferers demands a high bandwidth and a dynamic range for the ADC. Another requirement is for the analog circuits to be linear in order to prevent the intermodulation products of large interferers from disturbing the reception of a desired weak channel.

The bulk of signal processing, for example, interference attenuation, channel selection, digital demodulation, takes place in the digital domain. An advantage of handling channel filtering and demodulation functions in the digital domain is that this method leads to flexible multi-standard receiver architectures. Filters with sharp stop band roll-off and linear phase characteristics can be easily synthesized in the digital domain. However, since, in that case, the task of the digital filters, in addition to filtering the quantization noise, includes attenuation of the interfering signals, the situation calls for digital filters of higher complexity, which cause higher power dissipation. A possible way to reduce power dissipation would be to adapt the order of the digital filter to the levels of the interfering signals, for example, reduction of the filter order for low interfering signal levels. However, the required interferer power detection circuitry adds to the complexity of the receiver, and there can also be transition errors when the order of the filter is changed.

2.4.2 Filtering Interfering Signals in the Analog Domain

An analog filter at the input of an ADC may be used to attenuate the interferers, and the dynamic range and the linearity requirements of the ADC are thus relaxed. However, a serious drawback of the analog filters is the change of the filter characteristics due to process variations, and there can be differences between

identical circuits on the same chip- this can lead to mismatches and image issues in a receiver. There is a need for tuning or calibration to compensate for these process variations. The additional components add noise and distortion, which degrade the sensitivity of the receiver. Further, the signal quality at the input of the ADC can suffer due to the limited phase and pass band shape characteristics that can be implemented with analog filters. Unlike digital circuits, analog circuits do not scale well with technology migration and also lack the flexibility required for multistandard receivers.

2.4.3 Filtering Interfering Signals with a Filtering STF

An alternative solution is designing the signal transfer function (STF) of the ΔΣ ADC to provide a filtering transfer function. The ADC performs a filtering of the input signal before generating the corresponding digital output. The DSP performs high order filtering and channel selection at the ADC output. A filtering ADC relaxes the requirements of both the filtering in the IF path and the filtering in the digital domain. With a filtering STF, the ΔΣ ADC modulator reduces inter-modulation of the desired signal and the interfering signals at the input of the quantizer, and avoids the feedback of the high-frequency interfering signals at the input of the modulator. As will be shown in Chap. 3, ΔΣ modulator ADCs with filtering STF have significantly reduced intermodulation products caused by the feedback DAC non-linearities. Due to these reduced intermodulation products, ΔΣ modulator ADCs with filtering STF demonstrate higher SNDR for applications where the input signal is accompanied by strong out-of-band interfering signals.

The distributed feedforward and feedback (Fig. 2.9a, b) are two common topologies that have been successfully used to realize stable higher order ΔΣ modulators [12]. In the distributed feedforward topology the error signal fed into the loop filter consists primarily of quantization noise. The absence of signal component in the error signal results into reduced requirements on the loop filter linearity. These reduced linearity requirements enable reduction of the bias currents of the consecutive stages, and as a consequence makes feed forward architecture a low-power design. In comparison in the distributed feedback topology each integrator output contains a combination of filtered quantization noise and a large signal component to compensate for the average DC value of the quantizer feedback provided to each integrator. Keeping the integrator output swings within limits usually results in larger feedback integrator capacitors, and this increase in size tends to make the distributed feedback ΔΣ ADCs larger and more power hungry than circuits that use the feedforward architecture.

Fig. 2.10 shows NTFs and STFs derived for the fourth-order distributed feeedforward and feedback ΔΣ modulators shown in Fig. 2.9a and Fig. 2.9b. The transfer-function have been derived for a butterworth placement of the

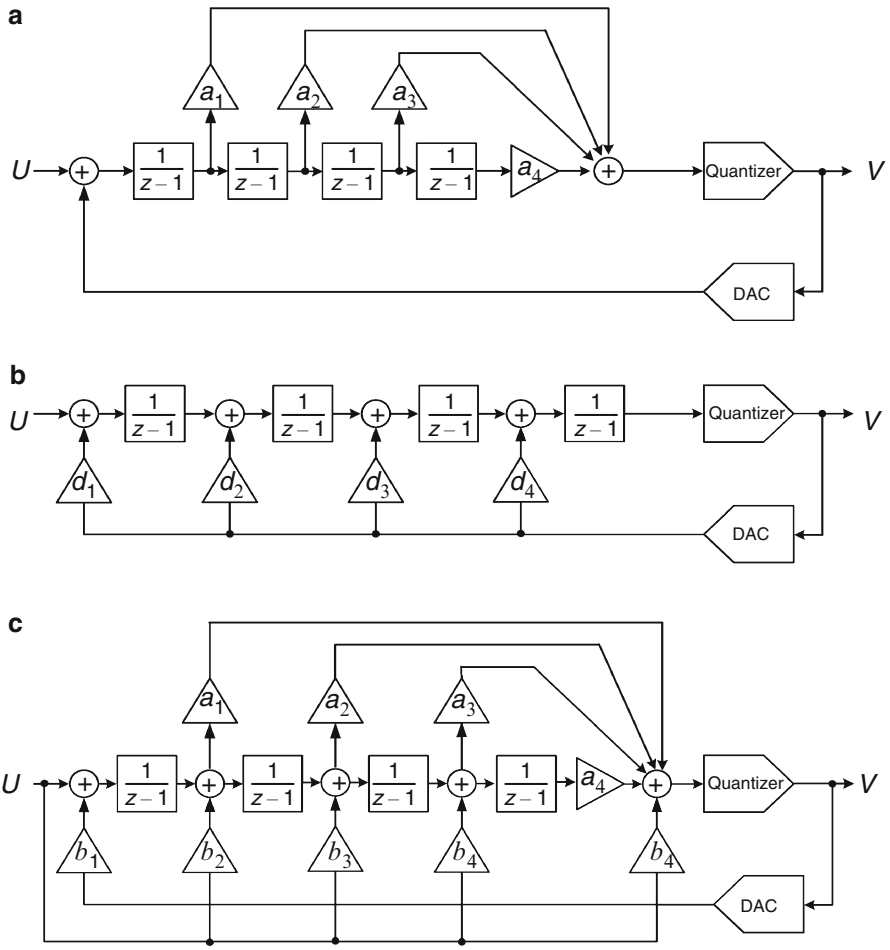


Fig 2.9 (**a**) ΔΣ modulators with distributed feedforward summation, (**b**) ΔΣ modulator with distributed feedback. (**c**) Modified distributed feedforward ΔΣ modulator with feed-ins to introduce STF zeros

transfer-function poles. The coefficients used in the derivations of these transfer-functions are:

$$a_1 = d_4 = 2.5535$$
$$a_2 = d_3 = 2.7446$$
$$a_3 = d_2 = 1.4212$$
$$a_4 = d_1 = 0.2923$$

The NTFs for the two architectures are identical, however, as is evident from Fig. 2.10b the STF of the feedforward ΔΣ modulator shows an out-of-band peaking.

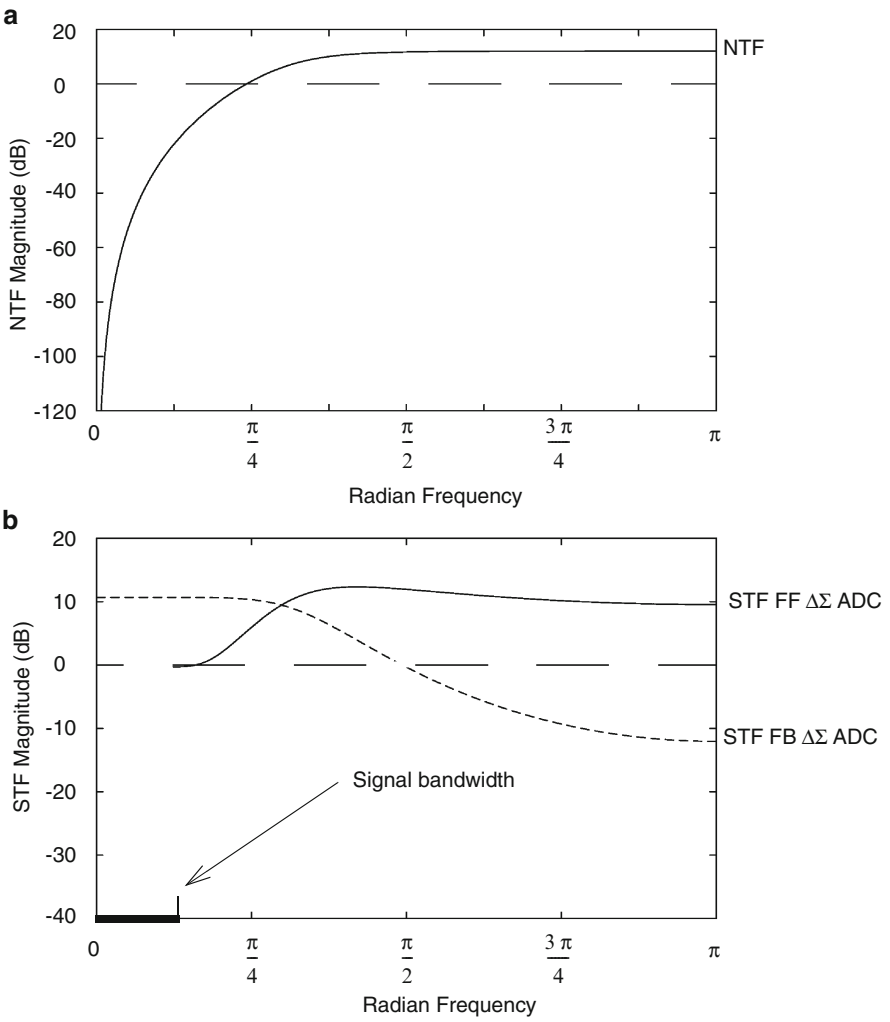


Fig. 2.10 NTFs and STFs for the ΔΣ modulators with distributed feedforward and distributed feedback: (**a**) NTF, (**b**) STF

The STF for the feedforward ΔΣ ADCs is flat within the signal conversion bandwidth, shows some overshoot for out-of-band frequencies, and provides first-order filtering beyond the unity-gain frequency of the loop. This out-of-band overshoot makes feedforward ΔΣ ADCs unsuitable for digitization of signal frequencies accompanied by high-frequency interferers. The out-of-band overshoot is caused by the STF zeros and implies that the out-of-band frequencies are amplified toward the output. This amplification means that the stable input range for out-of-band frequencies is smaller than that for the desired channel.

In comparison the STF of the distributed feedback ΔΣ modulator shows a lowpass filtering characteristic. The distributed feedback architecture results in an all-pole STF that does not contain significant peaking; as can be seen from Fig. 2.10b the STF may actually be a low-pass filter, which results in improved stability when it is driven by signals with significant out-of-band energy. However, the low-pass response of the STF for the distributed feedback architecture becomes significant at least one decade above the signal bandwidth, and that response makes its filtering ineffective for signals accompanied by adjacent channel interferers.

A possible way to control the out-of-band characteristics of the STF for the feedforward ΔΣ modulator is to insert zeros in the stopband region of the STF. For example, these zeros in the STF can be achieved by introducing feed-ins as shown in Fig. 2.9c. However, as will be demonstrated in Chap. 3, this independent designing of NTF and STF does not produce STFs with optimum out-of-band filtering characteristics. In Chap. 3 an NTF-STF co-design algorithm for designing of high SNR ΔΣ modulators with filtering STFs is proposed.

In [13], a combination of distributed feedback and feedforward topologies has been used to implement a ΔΣ ADC with a filtering STF. In the proposed architecture, a feedback coefficient in a fourth order distributed feedback architecture has been replaced by a feedforward path: d2 coefficient in Fig. 2.9b has been replaced by a feed-in coefficient c2 (refer to Fig. 2.11a). With a feedforward coefficient, it is possible to introduce a zero in the STF of the ΔΣ ADC, and this introduction allows attenuation of the interferers around the frequency band corresponding to the zero, refer to Fig. 2.11b. However, the value of the coefficient is bound to the NTF transfer-function. The zeros introduced also neutralize the STF poles, and thus reduce the higher-frequency filtering.

An alternative ΔΣ ADC topology based on feedforward architecture, with additional high-pass and low-pass filters in the feedback and forward paths, has been presented in [14]. The proposed architecture controls the STF's shape with a low-pass filter, H_{LP}, in the forward path. A high-pass filter, H_{HP}, has been introduced in the feedback path to compensate for the low-pass filter and thus retain the NTF shape; refer to Fig. 2.12.

However, the order of the low-pass filter implemented by the STF is limited by the low-pass filter introduced in the forward path, and the order can not be increased without impacting the loop filter noise and stability characteristics. The continuous-time ΔΣ ADC in [14] has been designed for the bluetooth signal bandwidth of 2 MHz, and the STF has been reported as a first-order low-pass filter with 3 dB bandwidth of 3 MHz.

A distributed feedback ΔΣ ADC with a filtering STF has been proposed in [15] (refer to Fig. 2.13). The ΔΣ ADC implements a notch in the STF stop-band by introducing a complex filter after the first integrator in the loop. However, the technique is limited to introducing STF zeros for selected interfering signals, and designing an STF mask for greater selectivity increases the complexity of the loopfilter and has impact on the stability of the modulator.

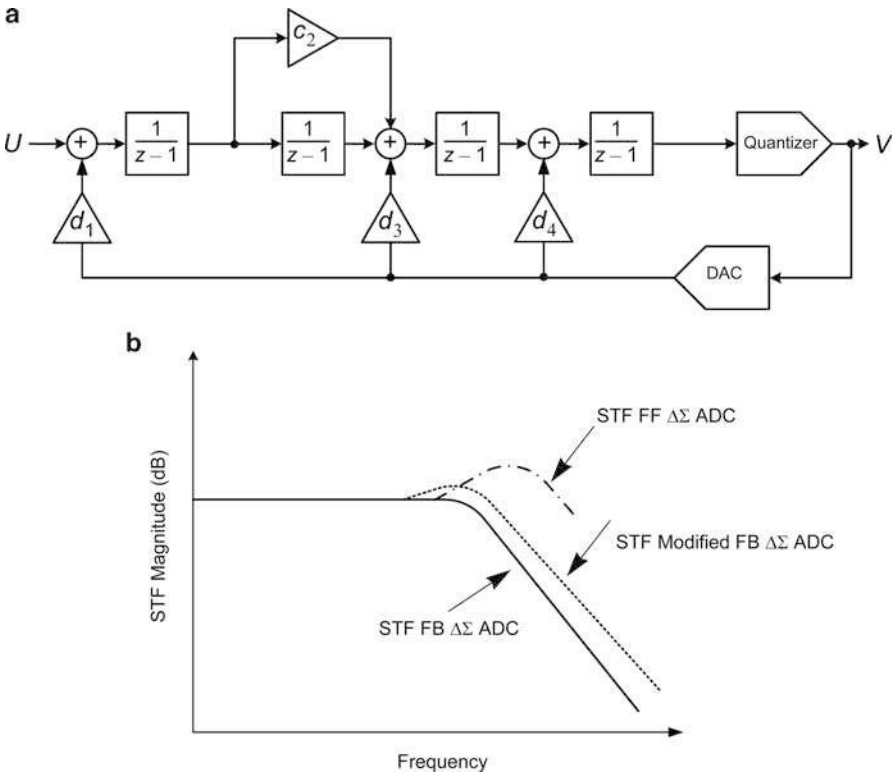


Fig. 2.11 (**a**) Modified feedback ΔΣ modulator [13], (**b**) STFs for the modulator architectures

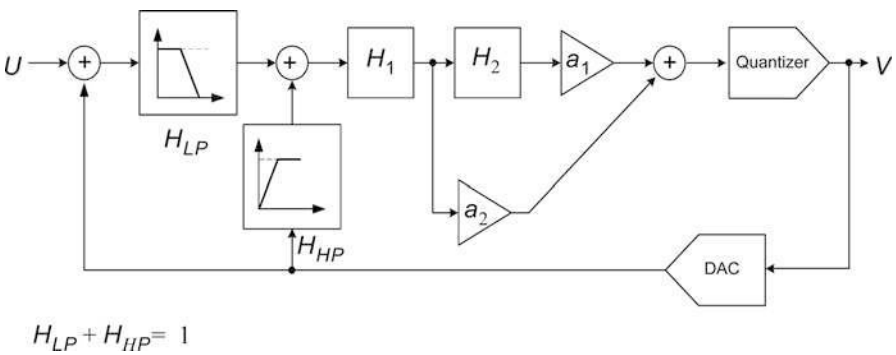


Fig. 2.12 ΔΣ modulator with additional low pass and high pass filters in forward and feedback paths to implement a filtering STF [14]

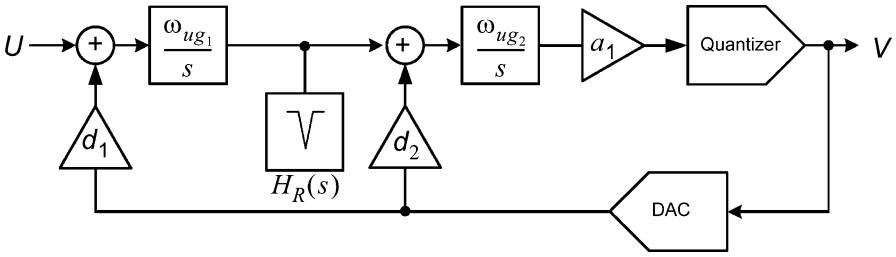


Fig. 2.13 ΔΣ modulator with a notch in the stopband to implement a filtering STF [15]

2.5 Specifications for a Complex ΔΣ ADC Used in a DTV Receiver

The proposed ΔΣ ADC has been designed for a low-IF receiver for ATSC and DVB-T digital TV standards. The digital TV signal bandwidth is approximately 6 MHz for ATSC and 8 MHz for DVB-T. At an OSR of 16, the sampling frequencies are 96 MHz and 128 MHz for ATSC and DVB-T respectively. The OSR value has been selected as a trade-off between the anti-alias filtering and the signal-to-noise ratio (SNR) requirements of the ADC. A third order complex bandpass filter, centered at 8 $\pm$ 2.4 MHz, and with 3 dB bandwidth of 24 MHz, meets the anti-aliasing requirements of the ADC; refer to Fig. 2.14.

Most of the conventionnal receiver architectures rely on analog filtering for rejecting interfering signals and use analog automatic gain control (AGC) to compensate for the wide dynamic range of the desired signal. The result is that usually a precise analog-to-digital conversion is not necessary, and the conversion rate can be as low as the symbol rate of the transmitted signal. For example, the bit detector in a DVB-T receiver requires only 27.5 dB of SNR to achieve the required 2×10^{-4} BER. Therefore, a pair of flash ADCs that each perform 5-bit uniform quantization sampling at Nyquist frequency would more than suffice in a DVB-T receiver that performs quadrature down-conversion, with all filtering and AGC in the analog domain. However, in integrated receivers, given the reduction in power consumption and circuit complexity that can be achieved by trading analog processing for digital processing, the trend is to perform as much of the signal processing as possible, e.g., channel selection etc., in the digital domain.

An advantage of this architecture is that the I/Q matching accuracy is very good, depending basically on the matching of the ADC input stage. In addition, as the filters are implemented digitally, they can have very accurate frequency response and linear phase characteristic, which are important for digital modulation techniques. However, this interchange of channel filtering and ADC greatly increases the dynamic range and sample-rate required of the ADCs. ADCs with a resolution of more than 13-bits are typically required. For example, DVB-T tuner sensitivity for a 8 MHz channel is approximately −95 dBm for the QPSK scheme and −75 dBm for QAM scheme. In the absence of any interference, the maximum

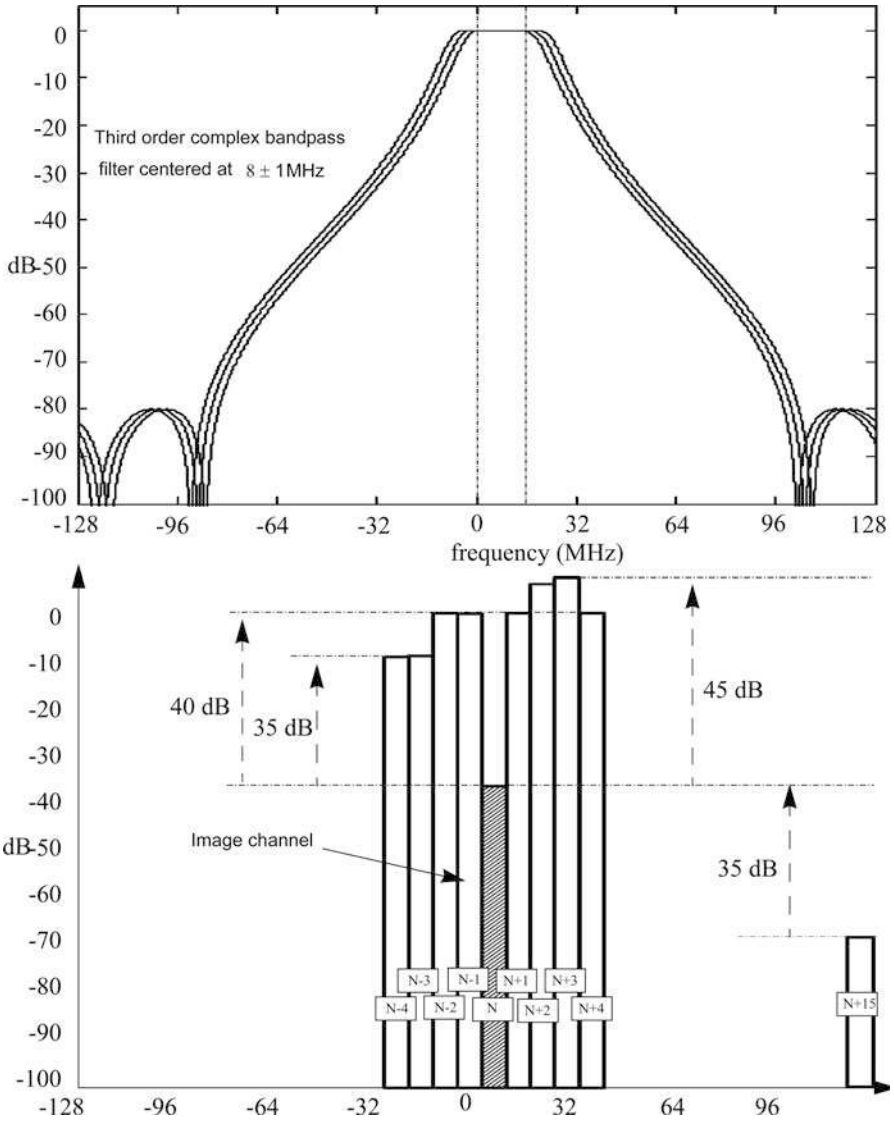


Fig. 2.14 The interfering signals for DVB-T with a third order complex bandpass filter at the input of the ΔΣ ADC

wanted DVB-T signal for the tuner input is −28 dBm. Therefore, considering −95 dBm sensitivity, the receiver has to provide at least a dynamic range of 67 dB.

The proposed low-IF receiver solution follows a variable gain amplifier (VGA) with automatic gain control (AGC) and ADC approach. By distributing the receiver specifications between VGA and ADC, both the circuits can be designed with reduced complexities. With the analog front-end filter implemented as a broadband

anti-aliasing filter, the SNR requirements of the ADC are decided by the required adjacent-channel immunity. The ADC samples signals comprising the desired signal, the image signal, and some adjacent signals.

The target SNR for the ADC has been determined in a way that is consistent with the following considerations:

- For ATSC, the required desired-to-undesired signal ratio (D/U) for the adjacent channel NTSC interference into the desired DTV channel is −40 dB [9]. For higher channels, the maximum rejection threshold for DTV interference into DTV has been set at −48 dB. When a carrier-to-noise ratio (C/N) of 15.5 dB is maintained, the required SNR of the ADC works out to be 63.5 dB.
- According to DVB-T standards, assuming 64-QAM and $CR = 3/4$, the adjacent channels ($N \pm 1$) can be up to 35 dB stronger, while the channels ($N \pm 2$) can be up to 43 dB stronger [10]. With the required carrier-to-noise ratio (C/N) of 27.5 dB for the reference BER in the Rayleigh channel (P_1), the dynamic range of the ADC is 62.5 dB. When an extra headroom of 9 dB [16] is added to avoid clipping of the OFDM signal due to peak to average ratio (PAR) variations, the SNR of the ADC is 71.5 dB.

The output of the ΔΣ ADC comprises the desired signal centered at the low-IF of 3 MHz or 4 MHz, depending on the DTV standard, the mirror signal, the interfering signals, and the noise-shaped quantization noise. The final image rejection, down-conversion, and baseband filtering are done with the DSP. The down-conversion to the baseband can be performed by a double quadrature multiplication of the ΔΣ ADC output with a quadrature IF signal [17]. This quadrature multiplication will down-convert the desired signal to the baseband, centered around DC; however, it will also upconvert the mirror signal to the baseband. Given the image resulting from the adjacent channel, an image rejection of 55.5 dB for ATSC and 62.5 dB for DVB-T is required of the digital down-converter. To have an image rejection of higher than 62.5 dB, the ΔΣ ADC needs at least 11 bits of resolution.

2.5.1 *Mismatch and Image Rejection Requirements of the Low-IF Complex ΔΣ ADC*

A complex ΔΣ modulator, like a complex filter suffers from mismatches in the I and the Q paths. Due to mismatches, signal or noise at the image frequency aliases into signal band of interest and this leads to the deterioration of the ADC SNR. Figue 2.15 is a block diagram of a complex ΔΣ modulator with a mismatch in gain elements between the I and Q paths of the modulator. In Fig. 2.15, the complex ΔΣ modulator shown includes a complex filter having a transfer function H(z), two quantizers, and two mismatched multipliers with multiplication coefficients

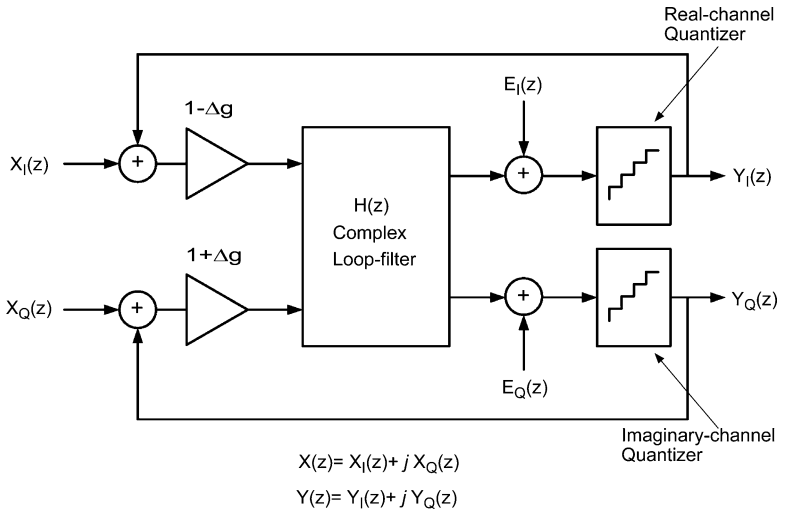


Fig. 2.15 A complex ΔΣ modulator structure with mismatch in gain elements

of $1-\Delta g$ and $1+\Delta g$. In the absence of mismatches ($\Delta g = 0$), the following equation is satisfied:

$$Y_I(z) + jY_Q(z) = \frac{H(z)}{1+H(z)}\big(X_I(z) + jX_Q(z)\big) + \frac{1}{1+H(z)}\big(E_I(z) + jE_Q(z)\big) \tag{2.11}$$

In the presence of mismatches between the gain elements ($\Delta g \neq 0$), (2.12) is satisfied.

$$\begin{aligned} Y_I(z) + jY_I(z) \;=\; & \frac{H(z) + (1-\Delta g^2)H^2(z)}{1 + 2H(z) + (1-\Delta g^2)H^2(z)}\big(X_I(z) + jX_Q(z)\big) \\ & + \frac{\Delta g H(z)}{1 + 2H(z) + (1-\Delta g^2)H^2(z)}\big(X_I(z) - jX_Q(z)\big) \\ & + \frac{1 + H(z)}{1 + 2H(z) + (1-\Delta g^2)H^2(z)}\big(E_I(z) + jE_Q(z)\big) \\ & + \frac{\Delta g H(z)}{1 + 2H(z) + (1-\Delta g^2)H^2(z)}\big(E_I(z) - jE_Q(z)\big) \end{aligned} \tag{2.12}$$

The last term represents the quantization noise in the image band aliasing into the signal band, and this process leads to the deterioration in SNR of the complex ΔΣ modulator. In [18], two more transfer functions – *image signal transfer function* (ISTF) and *image noise transfer function* (INTF) have been added to the existing two transfer functions – *signal transfer function* (STF) and

noise transfer function (NTF)- to describe the impact of mismatches in a complex ΔΣ modulator. In the presence of mismatches the output of the complex ΔΣ modulator can be written as [18]:

$$Y(z) = G(z)X(z) + \Delta G_{diff} X^*(z) + H(z)E(z) + \Delta H_{diff} E^*(z) \tag{2.13}$$

ΔG_{diff} is the *image* signal transfer function, or ISTF, which determines the gain from the image-signal input to the output, and ΔH_{diff} is the transfer function which determines the gain from the quantization-noise input to the modulator output. Though the in-band noise is shaped by the deep in-band notches of the NTF, the, image-band noise, which is significantly larger than in-band noise, is shaped by the INTF. The results is that mismatches cause out-of-band quantization noise in the complex ΔΣ modulator to alias into the in-band region. The INTF created by differential mismatch plays a critical role in determining the SNR of the non-ideal modulator. One of the techniques to reduce the differential error term ΔH_{diff} is to place one of the NTF notches in the quantizer's own image band; this method attenuates some of the image band noise, $E^*(z)$, before it aliases into the signal band [18]. However, the other differential error term, ΔG_{diff}, does not improve through the placement of the NTF notch in the image band, and strong interference at image frequency can be aliased into the signal band.

Given the strength of the adjacent channel interferers and the desired carrier-to-noise ratio, the image rejection requirements for the ΔΣ ADC work out to be 55.5 dB and 62.5 dB for ATSC and DVB-T standards respectively. Providing a safety margin to account for other noise sources which will degrade the SNR of the ADC, a ΔΣ ADC with a dynamic range of 75.0 dB, and image rejection better than 65 dB should be adequate for the digitization of the DTV signals in the proposed low-IF receiver.

References

1. S. Mirabbasi and K. Martin, "Classical and modern receiver architectures," *IEEE Communications Magazine*, Nov 2000, pp. 132–139.
2. Q. L. Liu, W. M. Snelgrove, and A.S. Sedra, "Switched-capacitor implementation of complex filters," *Proceedings of the 1986 IEEE ISCAS*, vol. 3, pp. 1121–1124, May 1986.
3. A. S. Sedra, W. M. Snelgrove, and R. Allen, "Complex analog bandpass filters designed by linearly shifting real low-pass prototypes," *Proceedings of the 1985 IEEE ISCAS*, vol. 3, pp. 1223–1226, June 1985.
4. R. H. Allen, "Complex analog filters obtained from shifted lowpass prototypes", M.A.Sc. thesis, University of Toronto, 1985.
5. S.A. Jantzi, K. Martin, and A.S. Sedra, "Quadrature bandpass DS modulation for digital radio," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1935–1949, Dec. 1997.
6. J. Crols, M.S.J. Steyaert, ''Low-IF topologies for high-performance analog front ends of fully integrated receivers," *IEEE Trans. Circuits Syst. -II: Analog and Digital Signal Processing*, vol. 45, no. 3, pp. 269–282, March 1998.

7. M. Hajirostam, K. Martin, ''On-chip broadband tuner design for cable modem and digital CATV,'' *48th Midwest Symposium on Circuits and Systems*, vol. 2, pp. 1374–1377, 2005.
8. I. Galton, "Delta-Sigma data conversion in wireless transceivers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50. no.1, pp. 302–315 Jan 2002.
9. *ATSC Recommended Practice: Receiver Performance Guidelines*, ATSC A/74, June 2004, pp 13–14.
10. *Mobile and Portable DVB-T/H Radio Access Interface Specification*, EICTA MBRAI-02.
11. G. Sgrignoli, C.W. Rhodes, "Interference mitigation for improved DTV reception," I*EEE Transactions on Consumer Electronics*, vol. 51, no. 2, pp. 463–470.
12. S. R. Norsworthy, R. Schreier, and G. C. Temes, Eds., *Delta-Sigma Data Converters: Theory, Design, and Simulation*. New York: IEEE Press. ISBN 0780310454.
13. F. Munoz, K. Philips, and A. Torralba, ''A 4.7mW, 89.5dB DR CT complex ΔΣ ADC with built-In LPF," *ISSCC Dig. Tech. Papers*, pp. 500–501, Feb., 2005.
14. K. Philips, P.A.C.M. Nuijten, R.L.J. Roovers, A.H.M. van Roermund, F.M. Chavero, M. T. Pallares, A. Torralba, ''A 2mW, 89dB DR continuous-Time ΔΣ ADC with increased wide-band interference immunity," *ISSCC Dig. Tech. Papers*, pp. 86–87, Feb., 2004.
15. Y. Le Guillou, and H. Fakhoury, ''Elliptic filtering in continuous-time sigma-delta modulator," *Electronics Letters*, vol. 41, no. 4, pp. 167–168, 17th Feb., 2005.
16. Hua Yu, Gang Wei, "Statistical distribution of the signal PAR in the practical OFDM systems," *International Conference on Communications, Circuits and Systems Proceedings*, vol 2, 25–28, June. 2006, pp. 1235–1239.
17. Chun-Huat Heng, Manoj Gupta, Sang-Hoon Lee, David Kang, Bang-Sup Song, "A CMOS TV tuner/demodulator IC with digital image rejection," *IEEE Journal of Solid-State Circuits*, vol 40, no.12, Dec. 2005, pp. 2525–2535.
18. S.A. Jantzi, K. W. Martin, and A. S. Sedra, "The effects of mismatch in complex bandpass ΔΣ modulators," *IEEE International Symposium on Circuits and Systems*, vol. 1, 12–15, May 1996, pp. 227–230.

Chapter 3
A Complex ΔΣ Modulator with an Improved STF

The presence of interferers puts a severe demand on the linearity requirements of the analog circuitry of a ΔΣ ADC and, in such applications, instead of unity signal-transfer functions (STF), it may be more desirable to have an STF with improved out-of-band attenuation. Depending on the application, e.g., single sideband (SSB), it may also be desirable to have higher attenuation in image band frequencies. Historically, complex transfer functions have been based on frequency transformations of real prototype filters. However, because of arithmetical symmetry, such complex transfer functions are inefficient in meeting the asymmetric requirements of a wireless receiver.

The design of an STF with higher stop-band attenuation has an implication for the quality of the noise-transfer function (NTF). This chapter discusses the trade-off involved in STF-NTF design.

The chapter further presents a methodology for designing arithmetically asymmetric complex signal-transfer functions and noise transfer functions that use complex filter routines [1] based on classical filter design procedures. A complex ΔΣ modulator architecture suitable for realizing the transfer functions that have been derived using the optimization is presented. The modulator and the design methodology have been used to design a prototype modulator for the DTV (ATSC and DVB) specifications. The advantages of the proposed ΔΣ modulator are presented.

3.1 ΔΣ Modulator Transfer Functions

A complex single-loop ΔΣ modulator can be modeled as a complex input linear block with arbitrary transfer functions, L_0 and L_1, from its two inputs, *U(z)* and *E(z)*, to the output (refer to Fig. 3.1) [2]:

$$NTF(z) = \frac{Y(z)}{E(z)} = \frac{1}{1 - L_1(z)} \tag{3.1}$$

B. Pandita, *Oversampling A/D Converters with Improved Signal Transfer Functions*, Analog Circuits and Signal Processing, DOI 10.1007/978-1-4614-0275-6_3,

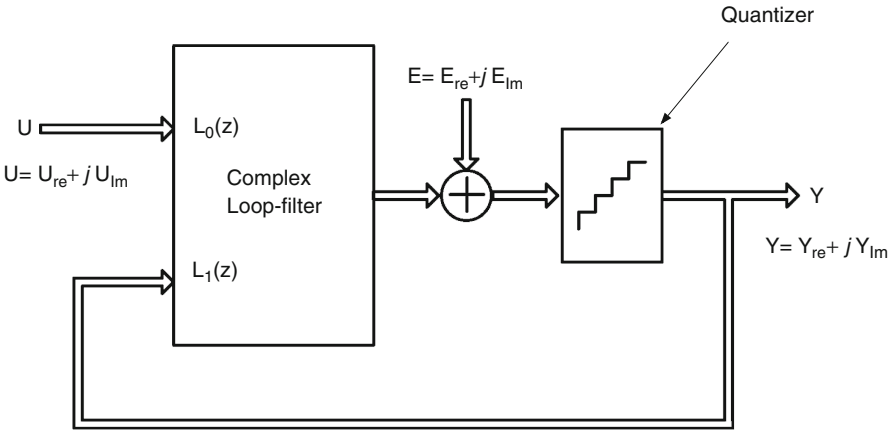


Fig. 3.1 A complex ΔΣ modulator structure

$$STF(z) = \frac{Y(z)}{U(z)} = \frac{L_0(z)}{1 - L_1(z)} \tag{3.2}$$

The double lines in the figure represent complex signals.

The design of a ΔΣ modulator typically starts with the selection of the NTF, which then defines $L_1(z)$ and hence the poles of the NTF and the STF. However, $L_0(z)$, which defines the zeros of the STF, can be chosen independently of the NTF, and this independence allows the design of modulators with non-flat signal transfer functions and stop-band attenuation characteristics controlled by the zeros of $L_0(z)$.

Figure 3.2 shows the structure of the proposed fourth-order complex ΔΣ modulator. The input feed-ins into each integrator stage set the four zeros of the fourth-order complex STF. The zeros of the complex NTF are set by the complex poles of the integrators, and a modulator with higher SNR over the signal bandwidth can be realized by distributing these zeros over the signal-band. The complex quantizer at the end of the channels (I and Q) of the modulator quantizes the complex analog-output signal and provide complex multi-bit output. The multi-bit outputs are feedback into the first stage of the modulator.

The loop transfer functions, $L_1(z)$ and $L_0(z)$, of the modulator are given by:

$$L_1(z) = -C_2\left(\frac{1}{z-p_1}\frac{z}{z-p_2}\frac{1}{z-p_3}\frac{z}{z-p_4} + \frac{B_1}{z-p_1}\frac{1}{z-p_3}\frac{z}{z-p_4} + \frac{(B_2 + B_3 z^{-1})}{z-p_1}\frac{z}{z-p_4}\right) \tag{3.3}$$

$$L_0(z) = -C_1 L_1(z) + F_1\frac{z}{z-p_2}\frac{1}{z-p_3}\frac{z}{z-p_4} + F_2\frac{1}{z-p_3}\frac{z}{z-p_4} + \left(F_3 z^{-1} + F_4\right)\frac{z}{z-p_4} \tag{3.4}$$

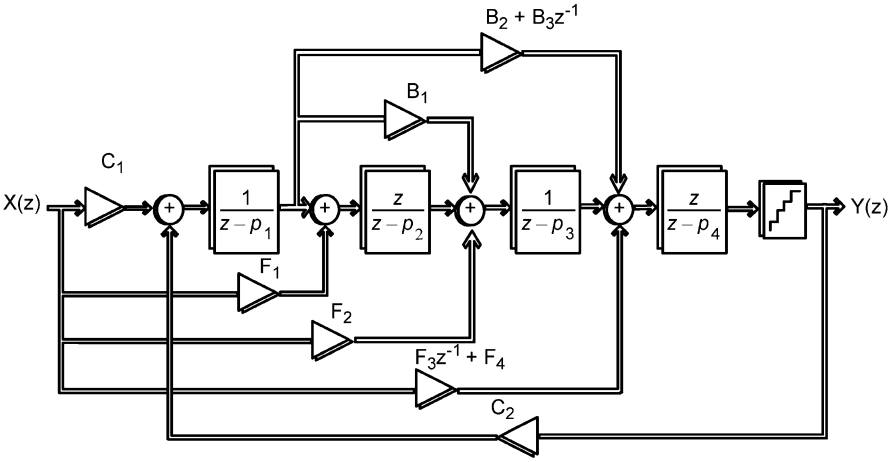


Fig. 3.2 Structure for the proposed fourth-order ΔΣ modulator with input feed-ins to realize zeros in the STF

From (3.4) and (3.2), it is evident that the input feedin coefficients (F) can be independently selected to define the zeros of the signal transfer function *STF(z)*. This property provides a freedom to design signal transfer functions with sharper transitions or with higher attenuation in specific stop-band regions.

A possible ΔΣ modulator design methodology could be to start with the design of the NTF and then use the feed-ins to control the STF zeros. The modulator coefficients can be derived by matching the STF and NTF with the desired transfer functions. However, an independent NTF and STF design disregards the inherent STF-NTF trade-off and implements either an STF with reduced stop-band attenuation or an NTF with degraded SNR. The next section discusses the trade-off involved in STF-NTF design.

3.2 NTF-STF Design Trade-Off

Filter approximation starts with the design of an input–output transfer function *H(jω)* that approximates an arbitrary shape *f(ω)* over the *jω* axis. For reasons of convenience, instead of *H(jω)*, the filter approximation uses the *characteristic function K(jω)*, which is defined this way [3]

$$H(j\omega)H(-j\omega) = 1 + K(j\omega)K(-j\omega)^{1} \tag{3.5}$$

[1] This equation is known in the literature as Feldtkeller's equation.

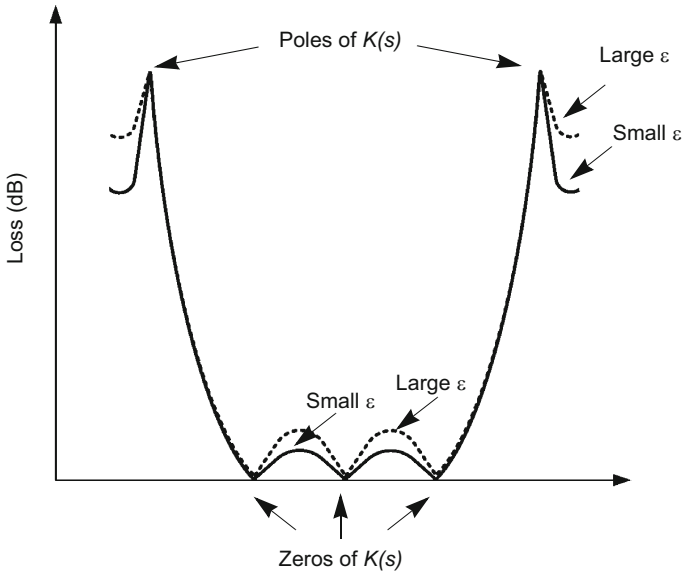


Fig. 3.3 Effect of ε on the attenuation characteristics of a filter

Attenuation of the filter network is given by

$$\begin{aligned} A(\omega) &= 10\ \log_{10} |H(j\omega)|^2 \\ &= 10\ \log_{10} \left(1 + |K(j\omega)|^2\right) \end{aligned} \tag{3.6}$$

By eliminating the unity constant, the filter approximation problem is reduced to the determination of the characteristic function *K(s)*. Thus, when *K(jω)* is infinite, the attenuation is infinite, and, when *K(jω)* is zero, the attenuation is zero (Fig. 3.3). The characteristic function can further be written as:

$$K(j\omega)K(-j\omega) = \varepsilon^2 \frac{F(j\omega)F(-j\omega)}{P(j\omega)P(-j\omega)} \tag{3.7}$$

The parameter 'ε' is referred to as the "passband ripple factor" [4]. From (3.7), it follows that, for given zeros and poles for *K(s)*, different values of the parameter 'ε' will result in different zeros for the transfer function *H(s)*. (refer to [4]).

The constraints imposed on the characteristic function are [1]:

- The zeros of *K(s)* lie in the pass-band, and
- The poles of *K(s)* lie in the stop-band region.

In terms of the zeros and poles of *K(s)*, the magnitude of *H(s)* for an odd order filter can be written as:[2]

$$|H(j\omega)|^2 = 1 + L^2 \left[\frac{\omega\left(\omega_{z1}^2 - \omega\right) \ldots \left(\omega_{zn}^2 - \omega\right)}{\left(\omega_{p1}^2 - \omega\right) \ldots \left(\omega_{pn}^2 - \omega\right)} \right]^2 \tag{3.8}$$

A similar expression can be written for an even order filter. A bilinear transformed variable (*Z*) is used to map the filter passband to the entire imaginary axis and the stopband to the finite positive-real axis. The transformed variable Z is related to the frequency variable *s* by the relation [3]:

$$Z^2 = \frac{s^2 + {\omega_B}^2}{s^2 + {\omega_A}^2} \tag{3.9}$$

As a result of this transformation, the pass-band region $(s = j\omega, \omega_A \leq |\omega| \leq \omega_B)$ of the *s*-plane is mapped to the entire imaginary *Z*-axis. The real frequencies $(s = \sigma)$ are mapped to the region $1 \leq Z \leq \omega_B/\omega_A$ of the real *Z*-axis. Similarly, the stop-band $(\omega > \omega_B \text{ or } \omega < \omega_A)$ and transition band are transformed to the real *Z*-axis [4]. Two of the advantages of carrying the filter design in terms of the transformed variable *Z* are that: (1) it simplifies the filter design expressions, and also (2) improves the numerical accuracy of the poles of *H(s)* near the passband edge by spreading the filter passband.

The trade-off involved in an STF-NTF design can be explained by considering an example of a filter design with poles of *K(s)*, which are placed using an iterative procedure as discussed in [1]. For an equiripple or maximally flat passband response the zeros of the characteristic function, *K(s)*, are defined explicitly by the poles of *K(s)*. In terms of the transformed variable *Z*, the characteristic function *K(s)* is given by:

$$K(Z)K(-Z) = \varepsilon^2 \frac{[(P(Z) + P(-Z))/2]}{P(Z)P(-Z)} \tag{3.10}$$

For a maximally flat passband, the characteristic equation is given by:

$$K(Z)K(-Z) = \varepsilon^2 \frac{\left(Z^2 + Z_0^2\right)^m}{P(Z)P(-Z)} \tag{3.11}$$

[2] The zeros of the transfer function *H(s)* are referred as natural modes, and, similarly, the zeros and the poles of the characteristic function are known as reflection zeros and loss poles in the filter design literature.

where

$$Z_0^2 = \left[\left(\frac{\omega_B}{\omega_A} \right)^{2NZ} \prod_{i=1}^{N} Z_i^4 \right]^{1/m}, \; m = NZ + NIN + 2N \tag{3.12}$$

Z_i is the transformed variable corresponding to the poles of *K(s)* on the imaginary axis $(s = j\omega)$; NZ = number of poles of *K(s)* at the origin; NIN = number of poles of *K(s)* at ∞; and N = number of poles of *K(s)* on the jω axis. The transfer function *H(s)* can be obtained by solving (3.5) and assigning the roots in the left-half plane to *H(s)*.

An insight into STF-NTF trade-off can be gained by considering a discrete fourth-order inverse Chebyshev filter with a monotonic passband and equiripple stop-band behavior designed for different values of the stopband attenuation parameter *L(=1/ε)*. The Feldtkeller equation for a fourth-order inverse Chebyshev filter with unity bandwidth and in terms of the continuous frequency variable s can be written as:

$$H(s)H(-s) = 1 + \frac{L^2}{V_4(s^{-1})V_4(-s^{-1})} \tag{3.13}$$

where V_4(s) is the fourth-order Chebyshev polynomial given by:

$$V_4(s) = 8s^4 - 8s^2 + 1 \tag{3.14}$$

The transformation from the continuous analog filter to a discrete filter with bandwidth ω_c can be done by the low-pass to low-pass transformation, written as (3.15), followed by the bilinear transformation, written as (3.16)

$$s \rightarrow \left(\frac{S}{\Omega} \right)_{\Omega = \frac{2}{T} \tan\left(\frac{\omega_c T}{2}\right)} \tag{3.15}$$

$$S \rightarrow \frac{2}{T} \frac{z-1}{z+1} \tag{3.16}$$

Figure 3.4 shows the magnitude plot of the fourth-order inverse Chebyshev filter versus ω for different values of the stopband parameter L. The case *L=0* corresponds to the degenerate case where the zeros of *H(s)* and the poles of the characteristic function *K(s)* cancel out each other exactly. Figure 3.5 shows the movement of the poles of the filter for increasing values of stopband attenuation. The figure makes it is evident that for higher stop-band attenuation of the low-pass filter, the filter poles crowd into the passband and stop-band transition region. A further insight into the movement of the filter poles can be gained by drawing a root locus plot of (3.13), with L(=1/ε) as the variable gain parameter. The zeros of

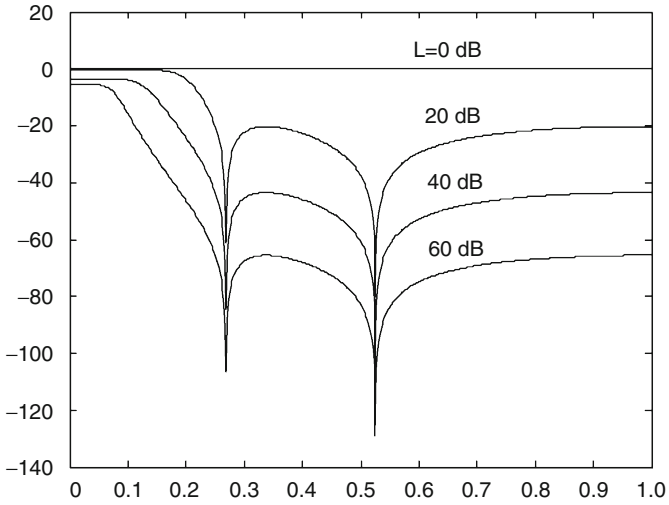


Fig. 3.4 Plot of the magnitude of the fourth-order Chebyshev filter for different values of the stop-band attenuation parameter L

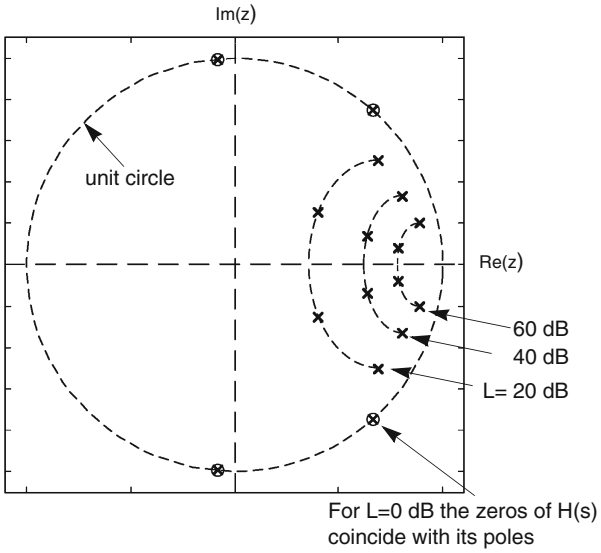


Fig. 3.5 Movement of the poles of H(s) for increasing values of the attenuation parameter L

H(s) are given by the points on the root locus branches for different values of L. The root locus branches start from the poles, ω_{pi}, of the characteristic function K(s) for $L \rightarrow 0$ and terminate on the zeros, ω_{zi}, for $L \rightarrow \infty$ (Fig. 3.6).

What this movement means is that, at increasing values of stopband attenuation, the zeros of *H(s)* move from the stop-band into the passband region. This movement

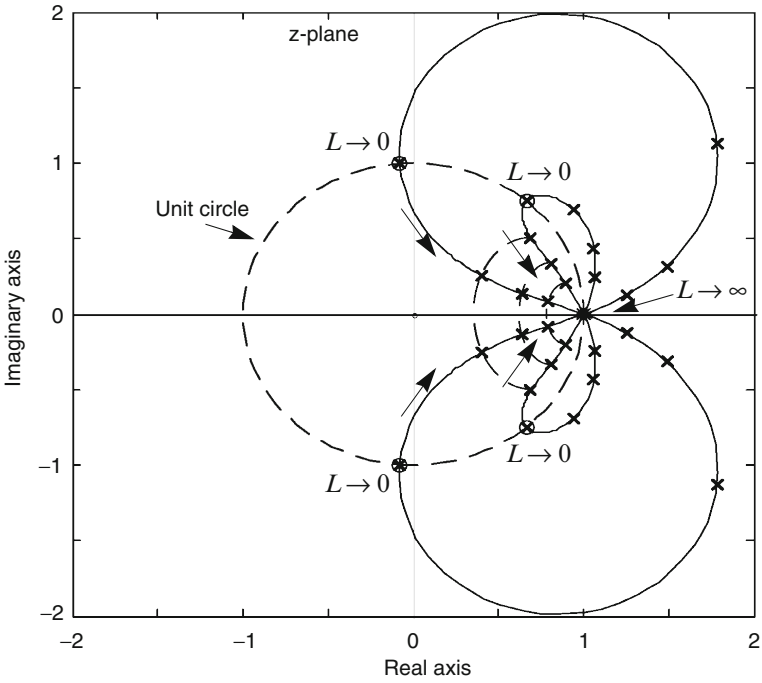


Fig. 3.6 Root-locus of the equation (3.8) as the filter attenuation, L, varies

of zeros of *H(s)* into the passband can cause partial or full cancellation of the zeros of the NTF and result in degradation of the NTF SNR at increasing values of the stop-band attenuation.

3.3 Background

3.3.1 The $|L|_1$ Norm and its Impact on the NTF Poles

The $|L|_1$ norm of an impulse response of a transfer function *H(z)* is given by:

$$|L|_1 = \sum_{n=0}^{\infty} |h(n)| \tag{3.17}$$

where *h(n)* is the impulse response of the transfer function *H(z)*. The $|L|_1$ norm has been used as a stability criterion in the design of delta-sigma modulators. Some of the other criteria used in the design of stable delta-sigma modulators are:

$$|L|_2 = \sum_{n=0}^{\infty} |h(n)|^2 \tag{3.18}$$

and

$$|H|_{\infty} = \max_{\omega} |H(e^{j\omega})| \tag{3.19}$$

Compared with the $|L|_2$ and $|H|_{\infty}$ norms, the $|L|_1$ norm is a stricter norm [5,6]. For a stable ΔΣ modulator, the upper and lower bounds on the quantization error accumulated at the input of the quantizer are given by:

$$\begin{aligned} e(n) &< \sum_{i=1}^{\infty} |h(n)| \frac{\Delta}{2} \\ &= (|L|_1 - 1) \frac{\Delta}{2} \end{aligned} \tag{3.20}$$

and

$$\begin{aligned} e(n) &> \sum_{i=1}^{\infty} |h(n)| \frac{-\Delta}{2} \\ &= -(|L|_1 - 1) \frac{\Delta}{2} \end{aligned} \tag{3.21}$$

Equations (3.20) and (3.21) assume that the quantization error is bounded between $-\Delta/2$ and $\Delta/2$, and, for an NTF, $h(0) = 1$. For an M-step quantizer to avoid overdriving the quantizer, the accumulated quantizer errors plus the peak-to-peak amplitude of the input, *u(n)*, should be less than the full-scale range, $(M + 1)\Delta$, of the quantizer. Hence, the worst case upper bound of:

$$|L|_1 = \frac{(M + 1)\Delta + \Delta - \max_n |u(n)|}{\Delta} \tag{3.22}$$

for the $|L|_1$ norm guarantees that the accumulated quantization errors do not exceed the stable input range of the quantizer and ensures the stability of the modulator.

The relation of the $|L|_1$ norm to the NTF gain and the poles of the NTF can be seen in Fig. 3.7. Figure 3.7a shows the magnitude response for a fourth-order NTF at different values of the $|L|_1$ norm. The NTF poles have been designed using the inverse Chebyshev function from the Matlab toolbox [7], and the NTF zeros have been independently distributed over the signal bandwidth. Figure 3.7a shows a pole-zero plot of the NTF poles and the corresponding values of the $|L|_1$ norm. From Fig. 3.7, the conclusion may be drawn that the $|L|_1$ norm increases as the NTF poles move away from the signal pass-band. This relation of $|L|_1$ norm to the NTF poles can be used to constrain the placement of the NTF poles and hence indirectly control the STF stop-band attenuation. This relation forms one of the constraints in the STF-NTF design optimization algorithm.

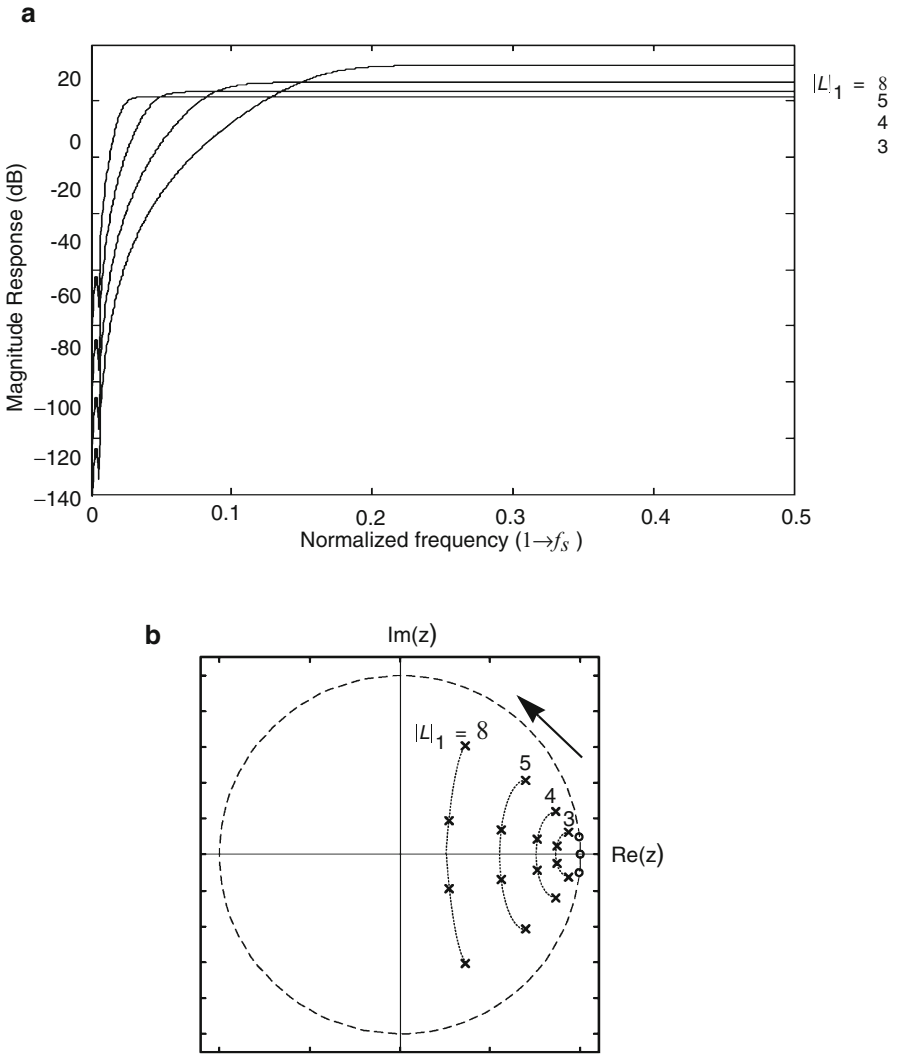


Fig. 3.7 (**a**) NTF magnitude for different values of the $|L|_1$ norm, (**b**) movement of the NTF poles with an increase in the $|L|_1$ norm

3.3.2 The Loss Function L(Z)

As discussed in Sect. 3.2, the poles of the characteristic function *K(s)* are constrained to be in the stop-band region, and the zeros are constrained to be in the passband region. By defining the poles of *K(s)* and the type of desired passband, it is possible to use simple formulae, as shown in (3.9) and (3.10), to directly

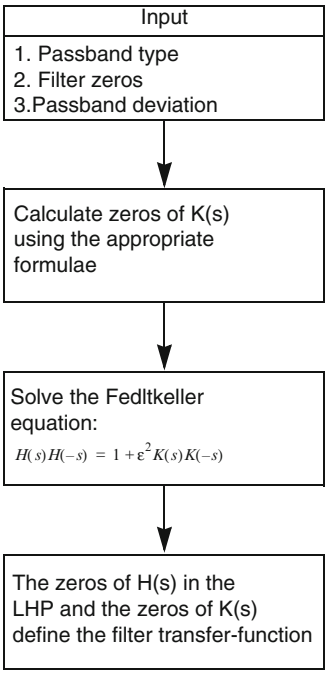


Fig. 3.8 A flow chart for filter designing with defined stop-band zeros and passband response type [4]

calculate the zeros of the characteristic function *K(s)*. These calculated zeros and the pre-defined poles can then be used in solving the Feldtkeller's equation and extracting the zeros of the input–output transfer function *H(s)*.

The approximation problem for filter design when the zeros of the filter and the desired passband response are defined can be solved by a computer program illustrated in the flowchart of Fig. 3.8. This solution means that, given the filter zeros, the passband deviation, and the passband type the filter transfer function can be determined. However, in actual filter design, the stopband zeros are not known, and the task of the computer program still remains to find them. It is possible to introduce a function, *L(Z)*, which, for an equiripple or maximally flat passband type, enables us to calculate the stop-band attenuation only in the terms of filter zeros. For a filter with an equiripple filter passband $\omega_A \leq \omega \leq \omega_B$ and with the following zeros:

- *NZ* zeros at the origin
- *N* finite zeros at $\omega_i (i = 1, 2, \ldots N)$
- *NIN* zeros at infinity

the loss function *L(Z)* is defined as

$$L(Z) = \left(\frac{Z + \omega_B/\omega_A}{Z - \omega_B/\omega_A}\right)^{NZ/2} \left(\frac{Z+1}{Z-1}\right)^{NIN/2} \prod_{i=1}^{N} \left(\frac{Z + Z_i}{Z - Z_i}\right) \tag{3.23}$$

where $Z_i^2 = \left(\omega_i^2 - \omega_B^2\right)/\left(\omega_i^2 - \omega_A^2\right)$.

For an equiripple passband filter, the stop-band attenuation is given by

$$A(\omega) = 10\ \log\left[1 + \frac{\varepsilon^2}{4}\left(|L| + \frac{1}{|L|}\right)^2\right] \tag{3.24}$$

A similar expression showing the stop-band attenuation only in terms of filter zeros can be found for a filter with maximally flat passband. The significance of this result lies in the fact that for a filter with an equiripple or maximally flat passband response the zeros of the filter uniquely determine the stop-band attenuation.

The filter approximation algorithm can now be described as:

- The poles of *K(s)* are iteratively modified to achieve the stop-band attenuation. This process of finding the optimum pole positions is known as pole placement. A modified Remez algorithm for pole placement has been described in [1].
- After achieving the optimum pole positions, the zeros of the characteristic function *K(s)* are obtained, as shown in (3.10) and (3.11).
- Finally, the Feldtkeller's equation (3.5) is solved in order to evaluate *H(s)*.

On the basis of this background information on the $|L|_1$ norm and its impact on the STF-NTF poles, and the pole placement algorithm that can be used for the optimum placement of zeros of the STF, the Sect. 3.6 describes an optimization algorithm for the STF-NTF co-design.

3.4 STF-NTF Co-Design Optimization Algorithm for the Design of Real ΔΣ Modulators

The STF-NTF co-design optimization algorithm for the design of lowpass ΔΣ modulator transfer functions can be described as [8]:

- The zeros of the STF are derived using the pole-placement algorithm described in [1].
- The Optimization algorithm proceeds with the minimization of the objective function, given by:

$$\int_0^{\frac{\omega_s}{2OSR}} |NTF(\omega)|^2 d\omega \tag{3.25}$$

Note the limits of the integral have been modified to correspond to the in-band noise for the lowpass case.

- The constraints for the minimization of the objective function are

  (a) the $|L|_1$ norm of the impulse response of the NTF.
  (b) the maximum radius for the NTF poles.
  (c) the maximum-deviation of the STF over the passband

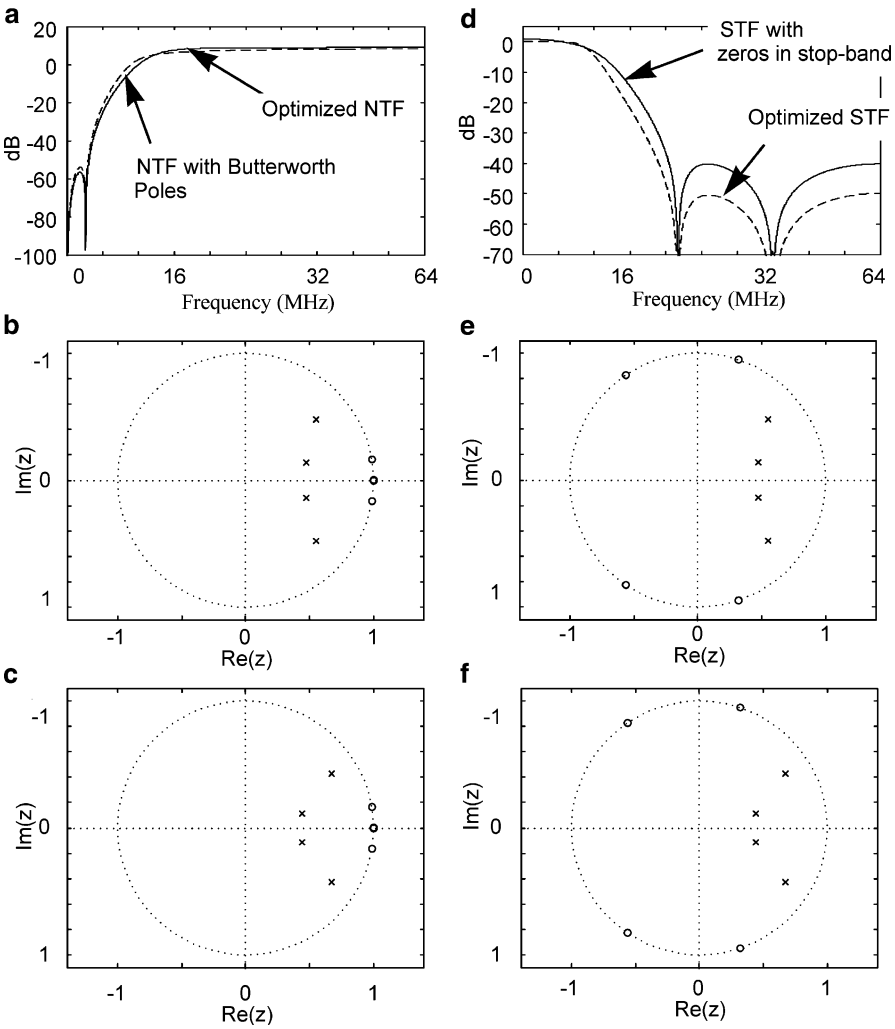


Fig. 3.9 Real Transfer functions for SQNR=88 dB. (**a**) NTF magnitude response, (**b**) pole-zero constellation for the non-optimized NTF, (**c**) pole-zero constellation for the optimized NTF, (**d**) STF magnitude response, (**e**) pole-zero constellation for the non-optimized STF, (**f**) pole-zero constellation for the optimized STF

An additional constraint on the complex poles and zeros of the NTF and STF is that they occur in complex conjugates. This limitation restricts the flexibility to place the complex poles and zeros in optimal positions:

NTFs, and STFs were derived for an SQNR of 88 dB and 101 dB. Figures 3.9 and 3.10 show the NTFs and STFs derived for a lowpass $\Delta\Sigma$ modulator for the following two cases:

1. The NTF and STF are derived independently. The transfer function design starts with an NTF that meets the required SQNR specifications, and the lowpass STF is obtained by inserting zeros in the stop band.

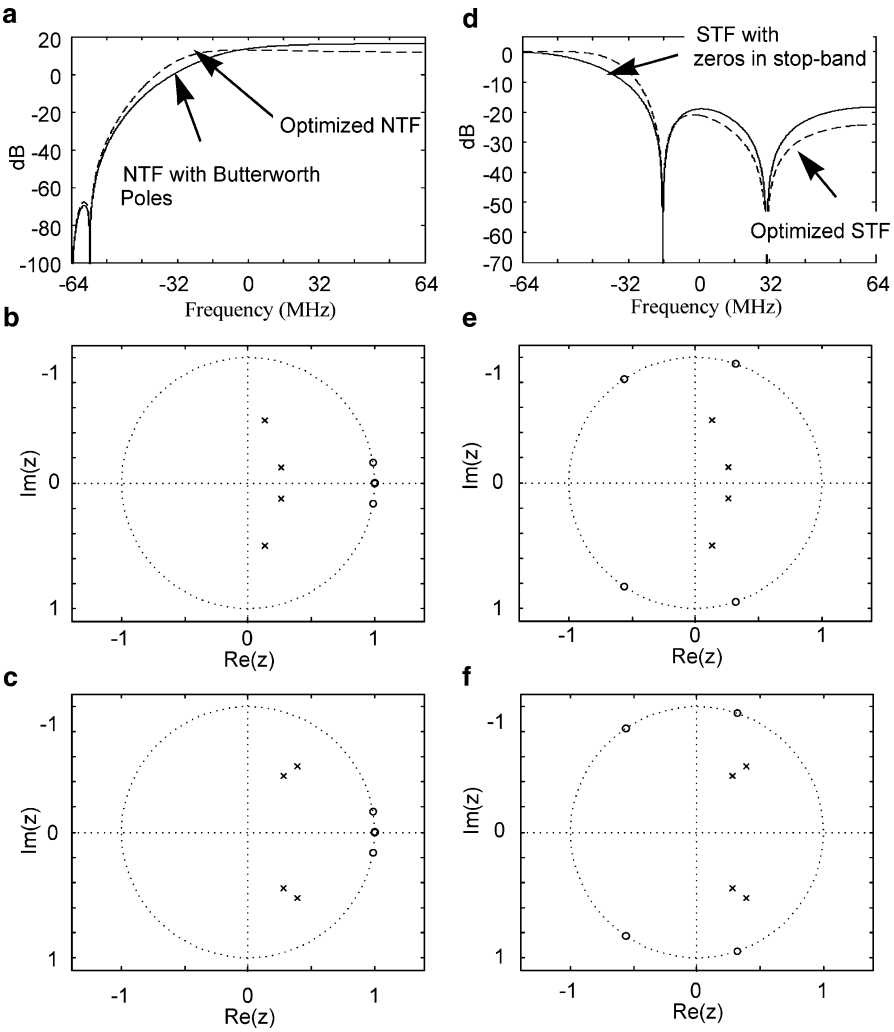


Fig. 3.10 Real Transfer functions for SQNR=101 dB. (**a**) NTF magnitude response, (**b**) pole-zero constellation for the non-optimized NTF, (**c**) pole-zero constellation for the optimized NTF, (**d**) STF magnitude response, (**e**) pole-zero constellation for the non-optimized STF, (**f**) pole-zero constellation for the optimized STF

2. The NTF and STF are co-derived employing the proposed algorithm. The algorithm starts with placement of the NTF and the STF zeros, and proceeds to the positioning of the transfer function poles.

As is seen from the Figs. 3.9 and 3.10 the NTFs derived by the by the proposed algorithm achieve the required SQNR, and the STFs have superior out-of-band rejection (refer to Table 3.1).

Table 3.1 SQNR vs. stop-band attenuation performance summary

Stop-band attenuation (dB)		
Optimized	Non-optimized	SQNR(dB)
25	20	101
50	40	88

3.5 Power and Performance Analysis of the Proposed Real ΔΣ Modulator

Figure 3.11 shows the ΔΣ modulator proposed in Sect. 3.1 modified to realize a low-pass ΔΣ modulator. The ΔΣ modulator architecture resembles a distributed feedforward architecture without input coupling [9]. The resonator formed by the last two delaying integrator stages and G_1 coefficient realize a pair of NTF zeros located at non-zero frequencies outside the unit circle, at $z = 1 + j\sqrt{G_1}$ [9]. Figure 3.12a shows the shape of the NTF designed for the proposed ΔΣ modulator. The NTF has been designed to realize an SQNR of 88 dB. A disadvantage of the architecture shown in Fig. 3.11 is that once the coefficients B_1, B_2, B_3, G_1, and C_2 have been decided to realize the optimum loop filter, the shape of the STF is fixed. As can be seen from Fig. 3.12b the STF for the selected loop-filter shape shows an out-of-band peaking. This out-of-band peaking can cause reduced input signal range and instability problem in presence of interfering signals. It is possible to control the shape of the STF by introducing zeros in the STF. In Fig. 3.13 the STF zeros have been realized by feeding input signal weighted by the feed-in coefficients, F_1, F_2, F_3, and F_4, to each integrator input.

The NTF for the architecture shown in the Fig. 3.13 is given by:

$$NTF(z) = \frac{1}{1 - C_2 L_1(z)} \tag{3.26}$$

where

$$L_1(z) = -B_3 I(z) + B_2 I(z) \frac{(z-1)}{(z-1)^2 + G_1} + B_1 I(z) \frac{1}{(z-1)^2 + G_1}$$

$I(z) = 1/(z-1)$ is the transfer function of the delaying integrator.

The STF for the architecture shown in the Fig. 3.13 is given by:

$$STF(z) = \frac{L_0(z)}{1 - C_2 L_1(z)} \tag{3.27}$$

where

$$L_0(z) = -C_1 L_1(z) + F_1 I(z) \frac{1}{(z-1)^2 + G_1} + F_2 \frac{1}{(z-1)^2 + G_1} + F_3 \frac{(z-1)}{(z-1)^2 + G_1} + F_4$$

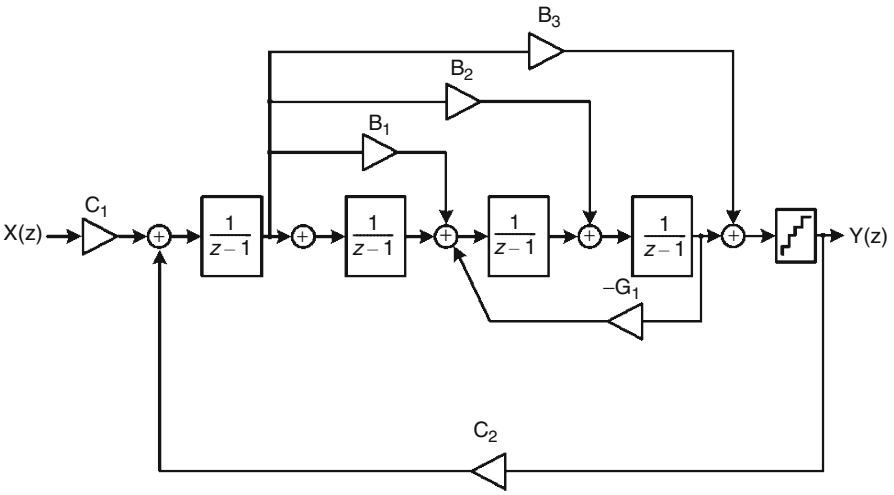


Fig. 3.11 The proposed ΔΣ modulator modified to realize a fourth-order real ΔΣ modulator

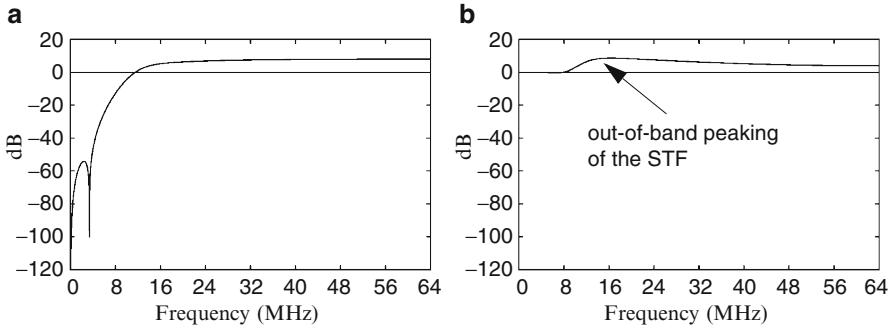


Fig. 3.12 The STF and NTF the proposed ΔΣ modulator without feed-ins: (**a**) NTF magnitude gain, (**b**) STF magnitude gain

An interesting choice for the feed-in coefficients is to make $C_1 = C_2$, $F_1 = F_2 = F_3 = 0$, and $F_4 = 1$. By the selection of these values for the feed-in coefficients the STF is equal to 1. Analysis of the input feedforward ΔΣ modulator architecture with unity STF reveals several advantages of the architecture:

- The input to the loop filter is given by:

$$X - Y = X - STF \cdot X - NTF \cdot E = NTF \cdot E \tag{3.28}$$

Thus the loop filter has to process quantization noise only. This results into reduced swings at the outputs of the integrators, which relaxes the headroom requirements of the opamps.

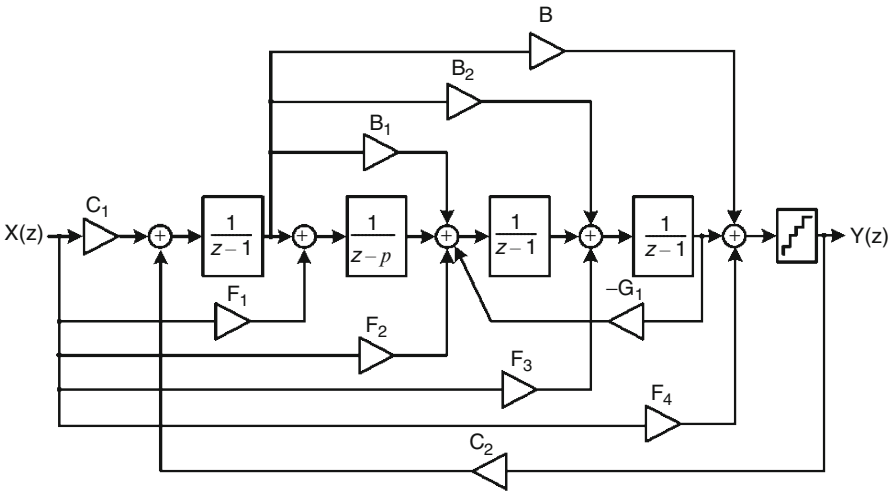


Fig. 3.13 The proposed ΔΣ modulator modified to realize a fourth-order real ΔΣ modulator with input feed-ins to realize zeros in the STF

- The distortion added becomes independent of the input signal, and this relaxes the linearity requirements of the analog blocks in the modulator.

A disadvantage of the input-feedforward architecture is that the feedforward introduces a delay-free loop starting from the input, through the quantizer, and finally through the DAC back to the input of the loop filter. This delay-free loop creates a speed path that complicates its implementation for high speed multi-bit modulators [10]. Also an active summation of the input signal and the loop filter output at the input of the quantizer increases the circuit complexity and power dissipation. An alternative technique of passive summation results into reduced signal level at the quantizer input, and hence demands comparators with higher resolution.

The proposed STF-NTF co-design optimization algorithm was used to design an NTF for an SQNR of 88 dB (OSR = 32), and an STF with low-pass filtering characteristics. Figure 3.14 shows the NTF and the low-pass filtering STF designed with the STF-NTF co-design optimization algorithm. A real ΔΣ modulator with the filtering STF (referred to as FADC in further discussion) and the NTF was implemented and compared to an input-feedforward ΔΣ modulator with the same NTF but with unity STF (referred to as FFADC in further discussion). The modulators were compared for power, and the impact of DAC and other coefficient mismatches on the modulator performance.

The ADCs were simulated in SIMULINK (Matlab) under the following conditions:

1. The αβγ representation [11] has been used to model the impact of finite dc gain of the opamp on the transfer function of an ideal integrator. The integrator model accounts for the finite dc gain and the output saturation voltages of the opamps.
2. The output saturation voltages of the integrators have been set at ±1.

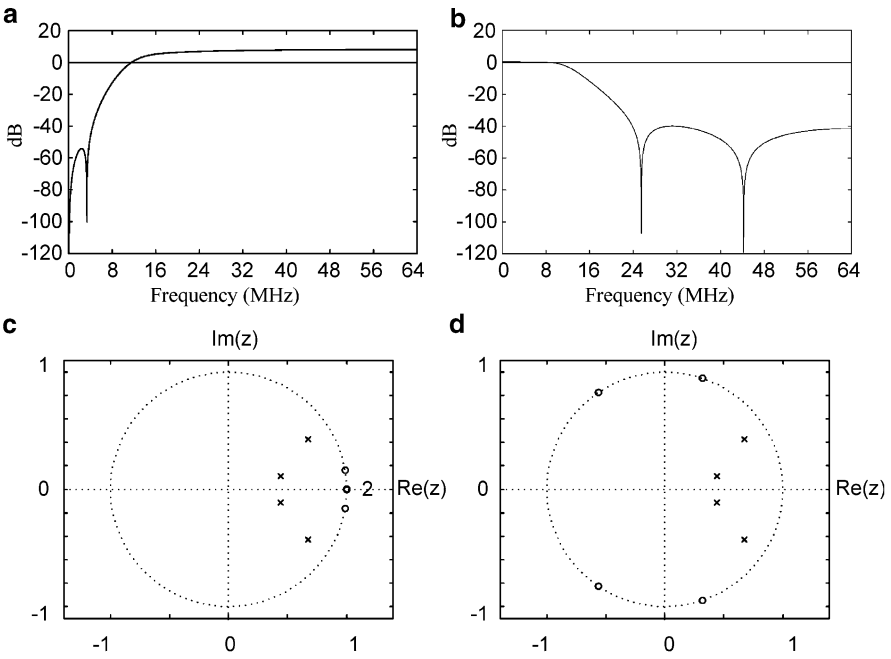


Fig. 3.14 The STF and NTF the proposed ΔΣ modulator with feed-ins to implement STF zeros: (**a**) NTF magnitude gain, (**b**) STF magnitude gain. Pole-Zero plot of: (**c**) NTF, (**d**) STF

3. Dynamic range scaling was performed to make the swings at the integrator outputs for the FFADC, FADC comparable.
4. A DAC mismatch of $\pm 0.5\%$ and $\pm 0.1\%$[3] was assumed to simulate for the impact of DAC non-linearity on the SNDRs of the ADCs.

3.5.1 Power Comparison

Figure 3.15 shows the signal swings at the integrator outputs for the feedforward modulator with unity STF (FFADC), which are estimated through the use of a histogram plot from the behavioral model simulation in Matlab. Figure 3.16 shows the histogram plots of the integrator outputs for the proposed real modulator with filtering STF (FADC). A comparison between Figs. 3.15 and 3.16 that the integrator swings for the modulator with unity STF are smaller; for example, for the first stage,

[3] For the selected process the standard-deviation (σ) for capacitor mismatch is given by $\sigma\% = \frac{1}{\sqrt{WL}}(appx.)$. Assuming the smallest realizable unit capacitor of dimensions $6\mu \times 6\mu$ yields $\sigma\% = 0.16$. Hence, for a 3σ design assuming a mismatch of 0.5% seems reasonable.

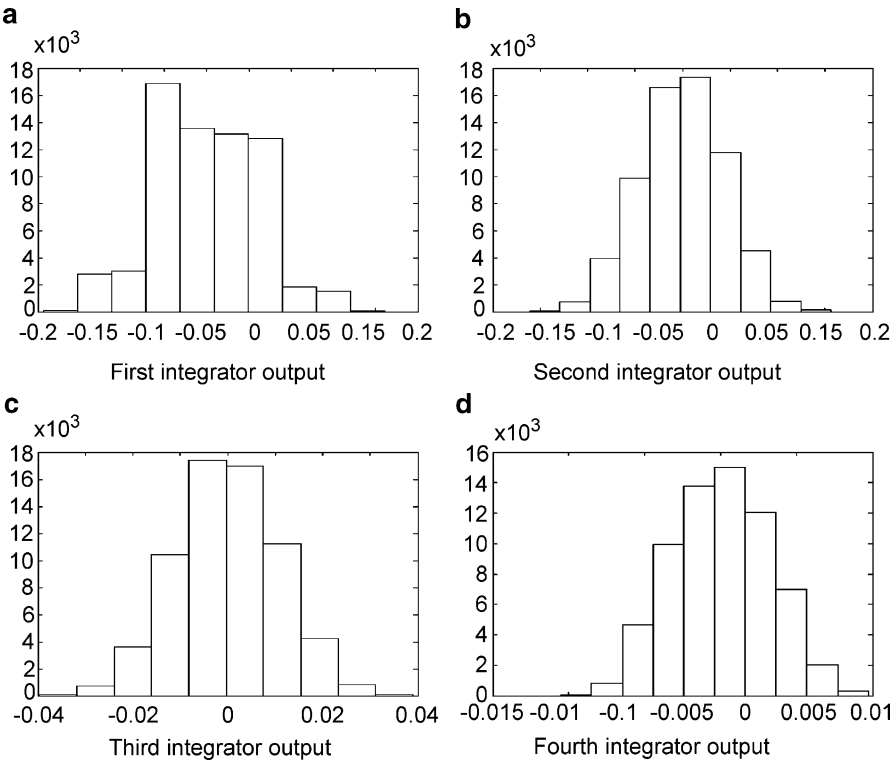


Fig. 3.15 Histogram plots of the integrator outputs for the modulator with unity STF (FFADC)

the output swings are about one-sixth of the proposed FADC and have higher distribution around the output common-mode. This difference in integrator swings means that, assuming that the same sampling capacitor sizes are constrained by noise considerations, dynamic range scaling [9] can be applied to make the integrating capacitors smaller in the Σ ADC with unity STF. This application results in reduction of the area of the chip.

3.5.2 Sensitivity to Intermodulation Due to DAC Non-linearity

ΔΣ modulators employ multi-bit quantization to meet the desired SNDR specifications. The advantages of the multi-bit quantization include 6 dB increase in the SQNR for every quantizer bit, the enhanced linearity of the feedback loop, and the relaxed slew rate requirement of the opamps in the loop filter. However, due to the device mismatches, the digital-to-analog converter (DAC) in the feedback path is inherently nonlinear. Error introduced by the DAC directly feeds to the input

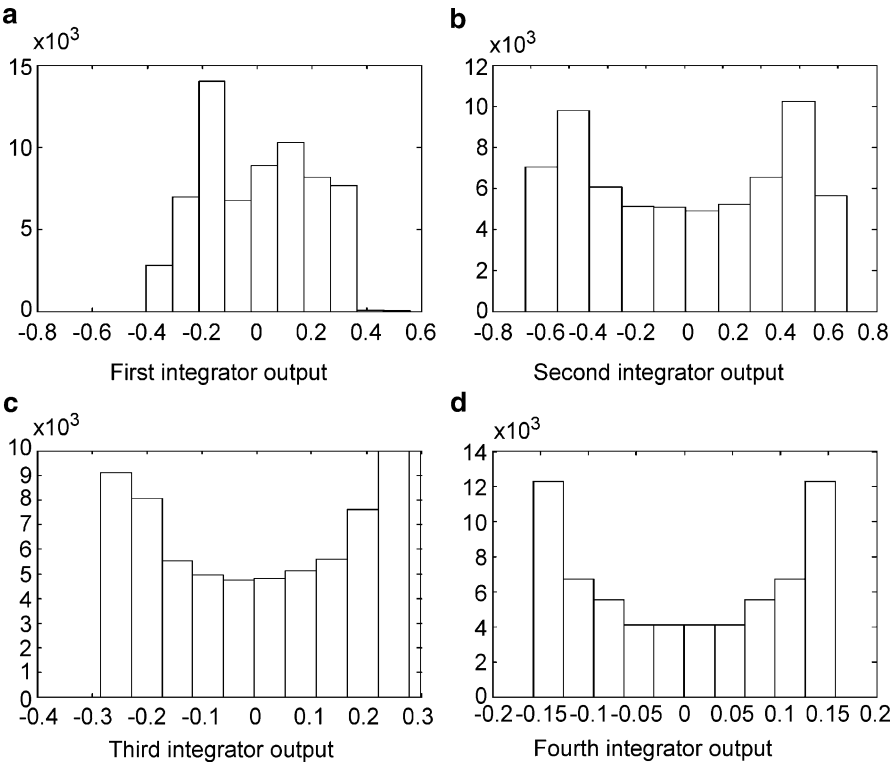


Fig. 3.16 Histogram plots of the integrator outputs for the modulator with filtering STF (FADC)

of the ΔΣ modulator. DAC non-linearity causes the high-frequency quantization noise to alias into the signal band, and results into the degradation of the SNDR of the modulator (refer to Fig. 3.17).

To determine the SNDR degradation of the modulators due to DAC mismatches, Monte Carlo simulations were run with a differential error ±0.5% and ±0.1% added to the DAC elements. The input to the modulators is a triple-tone consisting of: (1) –46 dBFS input at 4 MHz, (2) two interferers of strength −6 dBFS each at the frequencies of 24 MHz and 46 MHz respectively. Results from a set of 100 Monte Carlo simulations with DAC mismatches of ±0.5% and ±0.1% show that the SNDRs of the FFADC drops significantly and shows an SNDR (95th percentile) of 14.5 dB and 28.10 dB respectively. The FADC shows comparatively lower degradation in the SNDR and shows an SNDR (95th percentile) of 37.24 dB and 24.3 dB for the same DAC mismatches (refer to Table 3.5) (Figs. 3.18 and 3.19).

Table 3.2 summarizes the comparison between the proposed modulator with filtering STF and the feedforward modulator with unity STF for the test input (–46 dBFS desired signal at 4 MHz, two interfering signals of strength –6 dBFS each and at the frequencies of 24 MHz and 46 MHz respectively).

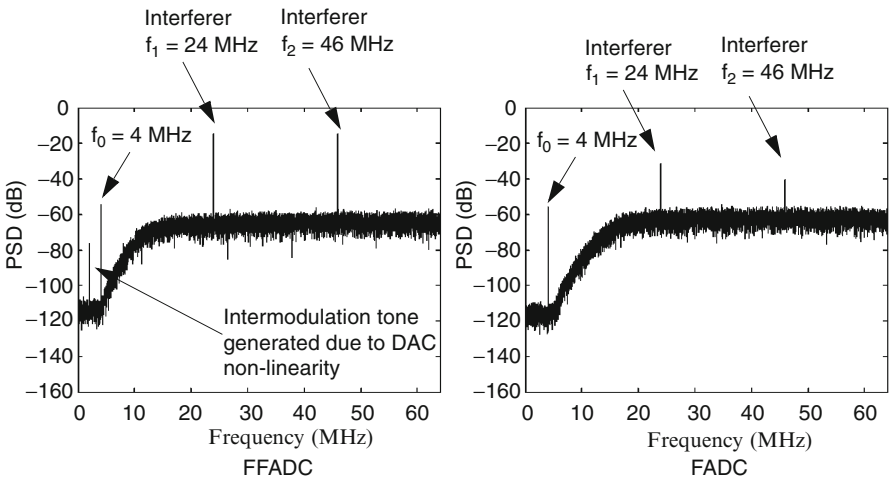


Fig. 3.17 Output PSD plot of the real ΔΣ modulators with DAC mismatch = ±0.5% for a weak desired signal (f_0) at −46 dBFS and strong interferers (f_1 and f_2) at −6 dBFS

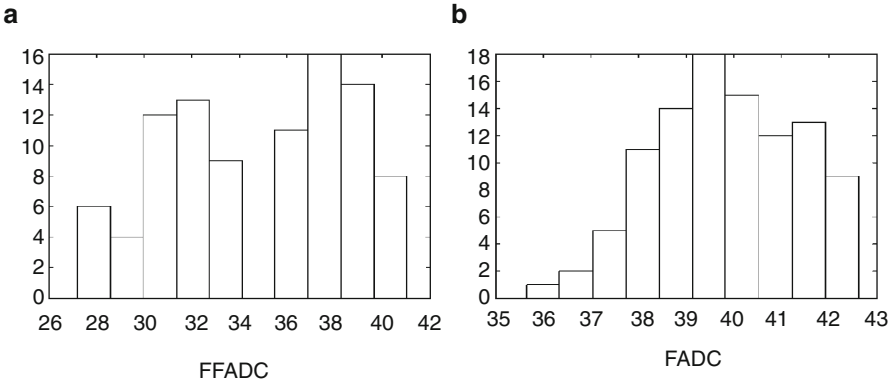


Fig. 3.18 Histogram plots of the SNDR for the FFADC and FADC for DAC mismatch = ±0.1%

The reason for the large degradation in SNDR for the feedforward ΔΣ modulator with unity STF can be understood by comparing the output PSDs for the two architectures. For the feedforward ΔΣ modulator with unity STF, the interfering tones at the output of the quantizer remain of the same magnitude as at the input (refer to Fig. 3.20).The large out-of-band quantization noise and the interfering tones are aliased back in-band due to the DAC non-linearity resulting into a severe SNDR degradation. Figure 3.21 shows the PSD at the output of the proposed real ΔΣ modulator. Due to the filtering nature of the ADC the interfering signals at the output of the quantizer are attenuated, and that

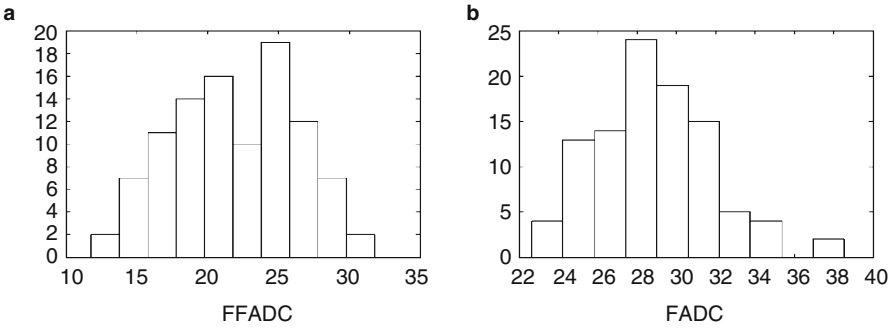


Fig. 3.19 Histogram plots of the SNDR for the FFADC and FADC for DAC mismatch = ±0.5%

Table 3.2 SNDR Comparison for the FFADC and FADC for DAC Mismatch

Modulator	$SNDR_{min}$	$SNDR_{max}$	SNDR[a]	DAC Mismatch
FFADC	27.22	41.03	28.10	±0.1%
FADC	35.65	42.62	37.24	
FFADC	11.75	31.80	14.5	±0.5%
FADC	22.65	38.54	24.3	

[a] 95^{th} Percentile

means reduced intermodulation products caused by DAC nonlinearities (refer to Figs. 3.22 and 3.23). This results into superior SNDR performance of the filtering ADC.

The two ADCs were compared for the impact of opamp dc gain variation and coefficient mismatch on SNDR performance. For an opamp dc gain variation from 80 dB to 40 dB both the architectures show an SNDR degradation of less than 0.5 dB. Similarly, for a coefficient mismatch of ±0.5% the two ADCs show an SNDR degradation less than 1 dB.

3.5.3 Stability Comparison

The proposed filtering ΔΣ modulator with optimized NTF poles was investigated for stability. Two types of modulators were designed with a peak NTF gain of 12 dB. One modulator was built with NTF poles arranged in butterworth order, and the second modulator was designed with NTF poles optimized by the STF-NTF co-design algorithm. The ΔΣ modulator with optimized NTF poles behaves well for inputs up to full-scale and reaches a peak SNR of 88 dB. The modulator with NTF poles arranged in butterworth order does not show any stability advantage over the modulator with optimized NTF poles.

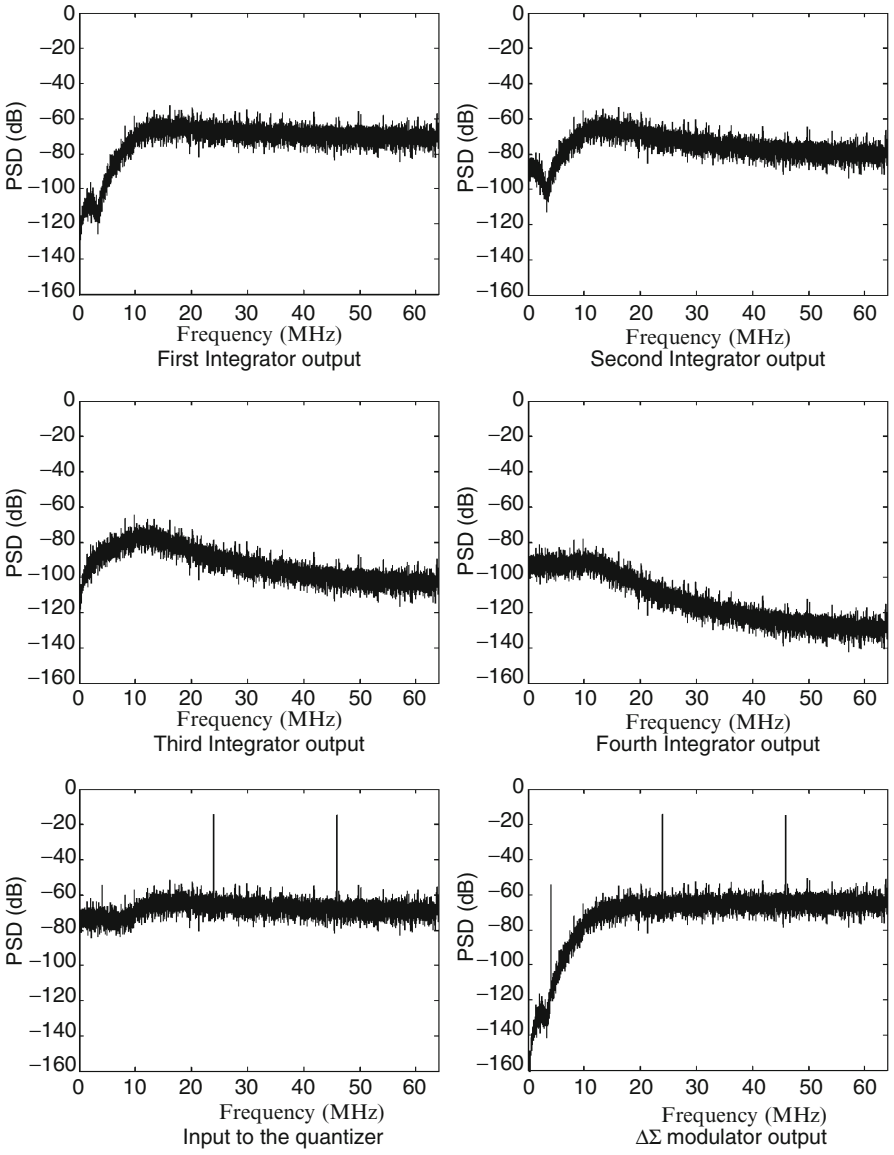


Fig. 3.20 PSD plots at the integrator outputs for the feedforward ADC with unity STF (FFADC)

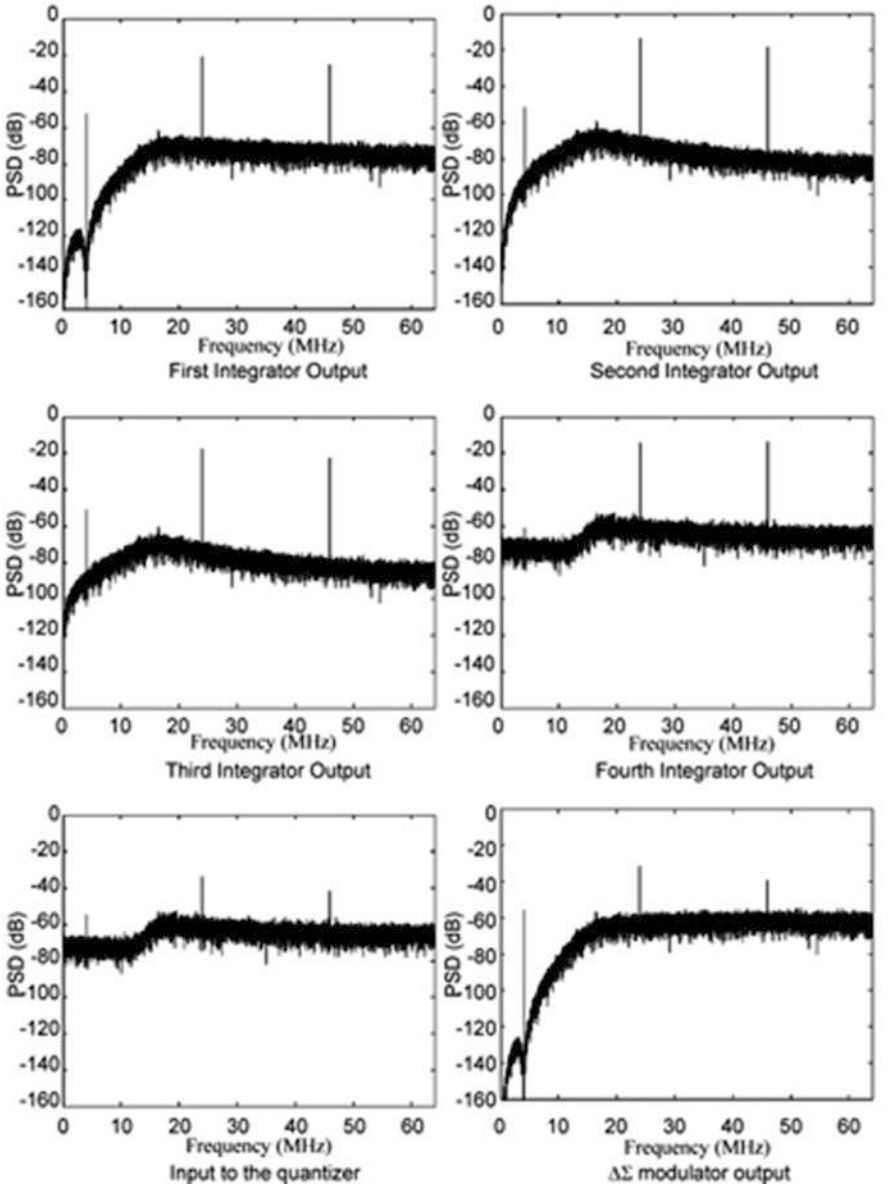


Fig. 3.21 PSD plots at the integrator outputs for the ADC with filtering STF (FADC)

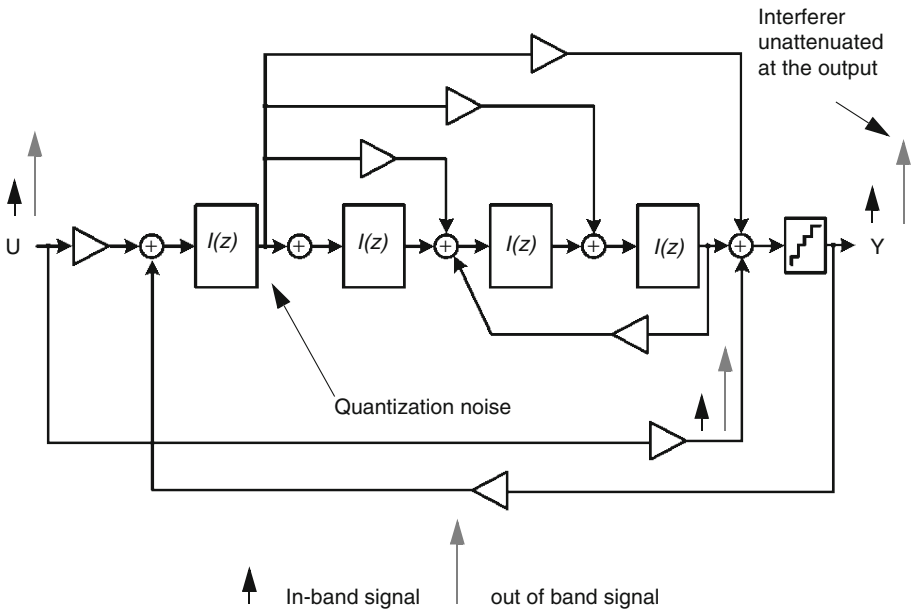


Fig. 3.22 Response of the feedforward ΔΣ modulator ADC with unity STF to an in-band signal and out of band interferer

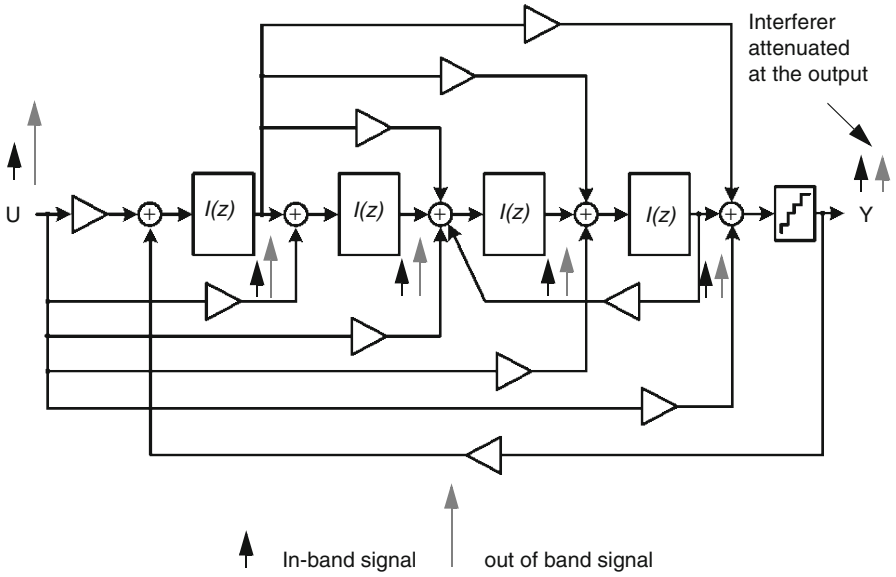


Fig. 3.23 Response of the feedforward ΔΣ modulator ADC with filtering STF to an in-band signal and out of band interferer

3.6 The STF-NTF Co-Design Optimization Algorithm for the Design of Complex ΔΣ Modulators

It is possible to derive complex transfer functions from the real prototypes by performing a simple frequency translation of the filter [25]. The real prototype filter symmetric about the dc is transformed into a non-zero IF complex filter symmetric about the IF. However, a disadvantage of complex filters derived this way is that they are arithmetically symmetric. Sometimes, it maybe desirable, for example, SSB modulation or demodulation, to derive complex filters with asymmetric specifications. With the background knowledge developed in Sect. 3.3, the optimization algorithm for an STF-NTF co-design for a complex ΔΣ modulator can now be described as [8]:

- The zeros of the STF are derived using the pole-placement algorithm described in [1];
- The Optimization algorithm proceeds with the minimization of the objective function, given by:

$$\int_{\omega_{IF}-\frac{\omega_S}{2OSR}}^{\omega_{IF}+\frac{\omega_S}{2OSR}} |NTF(\omega)|^2 d\omega \tag{3.29}$$

- The constraints for the minimization of the objective function are:

  (a) The $|L|_1$ norm of the impulse response of the NTF *NTF(z)*.
  (b) The maximum radius for the NTF poles.
  (c) The maximum-deviation of the STF over the passband

A fourth-order complex delta-sigma modulator was designed for the DTV receiver specifications for the DVB and ATSC [12,13]. To avoid issues such as dc-offset that are related to Zero-IF, the IF has been set at BW/2 (where BW corresponds to the signal bandwidth for the particular standard). For example, for ATSC and DVB DTV standards with signal bandwidths of 6 MHz and 8 MHz respectively, the IF has been set at a value of 3 MHz and 4 MHz respectively. For a maximum signal bandwidth of 8MHz, the sampling frequency has been set at a value of 128 MHz, which corresponds to an over-sampling ratio of 16.

In the first version of the modulator, the NTF zeros were distributed over the signal bandwidth. In a second version, three of the NTF zeros were distributed over the signal bandwidth and the fourth zero has been placed at the image frequency in order to reduce the aliasing of image-band noise into the in-band region of the modulator [14]. Sacrificing one of the NTF zeros degrades the signal-band quantization noise shaping of the modulator, but it results in a modulator with higher immunity to coefficient mismatches. The topic is further discussed in Chap. 4. For the DTV receiver application, it is advantageous to design an asymmetric complex STF with greater attenuation in the image band. An advantage of complex

transfer functions not designed by a simple frequency shift of the real lowpass prototype filters lies in the fact that they can be designed to meet these asymmetric requirements optimally.

The algorithm starts with an initial STF zero placement derived using [1] and then proceeds with the minimization of the objective function (refer to (3.29)). Through application of an iterative procedure involving fixed and moveable zeros of the transfer function, which is a feature allowed by the complex filter approximation routines, it is possible to experiment with different stop-band attenuations and the STF-NTF design. Figure 3.24 shows the NTF and the STF, which have been designed using the optimization algorithm for $|L|_1 = 3.5$. With help of Mathematica, the transfer-functions were mapped to the modulator coefficients shown in Fig. 3.2. Figure 3.24b shows the asymmetric filtering STF. The STF achieves a stop-band rejection of greater than 40 dB and 60 dB for the positive and negative frequencies respectively. Figure 3.24e shows a 64k-bin output spectrum of the modulator simulated in Matlab. With a 15-level DAC and at a sampling frequency of 128 MHz, the complex $\Delta\Sigma$ modulator achieves an SNDR of 55 dB for a –3 dBFS tone input frequency of 4 MHz.

Figure 3.25 also shows the NTF and the STF designed using the optimization algorithm for different values of the $|L|_1$ norm. Some of the things that can be observed from the figure are:

- Increasing the $|L|_1$ norm causes the NTF gain and the NTF attenuation to increase.
- Increasing the $|L|_1$ norm degrades the stop-band attenuation of the STF.

After mapping the transfer-functions to the modulator coefficients, a set of simulations were performed in order to observe the SNDR of the modulator. Table 3.3 summarizes the modulator performances for different signal and noise transfer functions generated using the optimization algorithm. The transfer functions derived for the norm value of $|L|_1 = 6.5$[4] have been selected for the implementation of the proposed $\Delta\Sigma$ modulator.

Figure 3.26a, b show the NTF and the STF selected for the proposed complex $\Delta\Sigma$ modulator. The modulator achieves an SNDR of 80 dB for a –3 dBFS tone input frequency of 4 MHz.

A set of fourth-order real NTFs was designed to meet a list of SQNR specifications of 101 dB, 94 dB, and 89 dB. The real NTFs were designed for a signal bandwidth of $\pi/16$ radians and an OSR of 16 (In terms of frequency this could correspond to a signal bandwidth of 4 MHz and sampling frequency of 128 MHz). The zeros of the NTF were distributed over the signal band, and the poles are placed in the butterworth configuration. It is possible to constrain the NTF pole position by specifying the out-of-band NTF gain. The lowpass transfer functions

[4] By using the modulator stability condition derived in (3.22), the case $|L|_1 = 6.5$ corresponds to an input signal more than 65% of the quantizer range, whereas the case $|L|_1 = 7.5$ corresponds to an input signal less than 60% of the quantizer range.

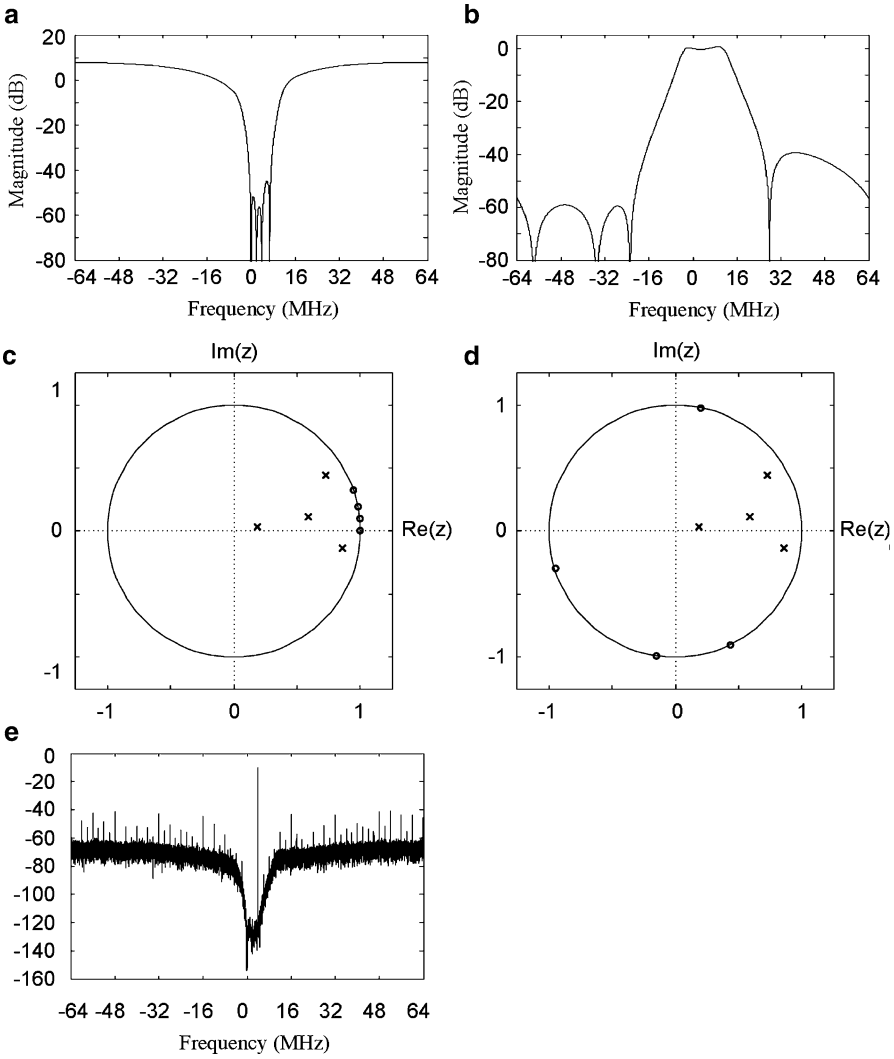


Fig. 3.24 Design of the STF-NTF using the optimization algorithm for $|L|_1 = 3.5$: (**a**) NTF magnitude gain, (**b**) STF magnitude gain, (**c**) NTF pole-zero plot, (**d**) STF pole-zero plot, (**e**) PSD plot of a complex ΔΣ modulator with STF and NTF transfer-functions as shown in (**a**) and (**b**)

were frequency shifted to an angular frequency of $\pi/16$ (4 MHz) to realize complex transfer functions. The frequency shift was implemented by multiplying all NTF poles and zeros by $e^{j(\pi/16)}$. As a result of the frequency shift the poles and zeros of the NTF have no complex-conjugates and the magnitude response is not symmetric about dc. The STF shares poles with the NTF. To realize a complex filtering STF zeros were inserted in the stop band region of the transfer function. To evaluate the efficacy of the optimization algorithm, a set of complex NTFs and STFs were

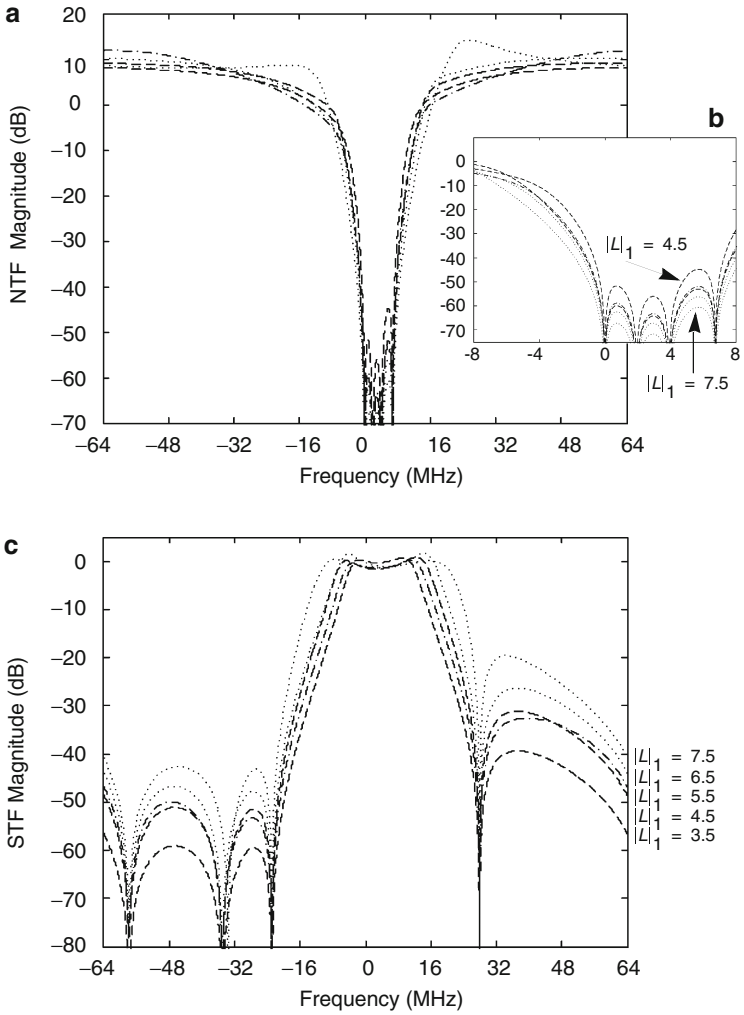


Fig. 3.25 NTF and STF designed for different values of the $|L|_1$ norm: (**a**) NTF magnitude plot, (**b**) in-band zoom-in of the NTF, (**c**) STF magnitude plot

Table 3.3 NTF-STF performance summary

	Stop-band attenuation		
$\|L\|_1$norm	-ve frequency	+ve frequency	SNDR (dB)
3.5	60	40	55
4.5	50	34	71
5.5	50	32	74
6.5	46	26.5	80
7.5	40	20	85

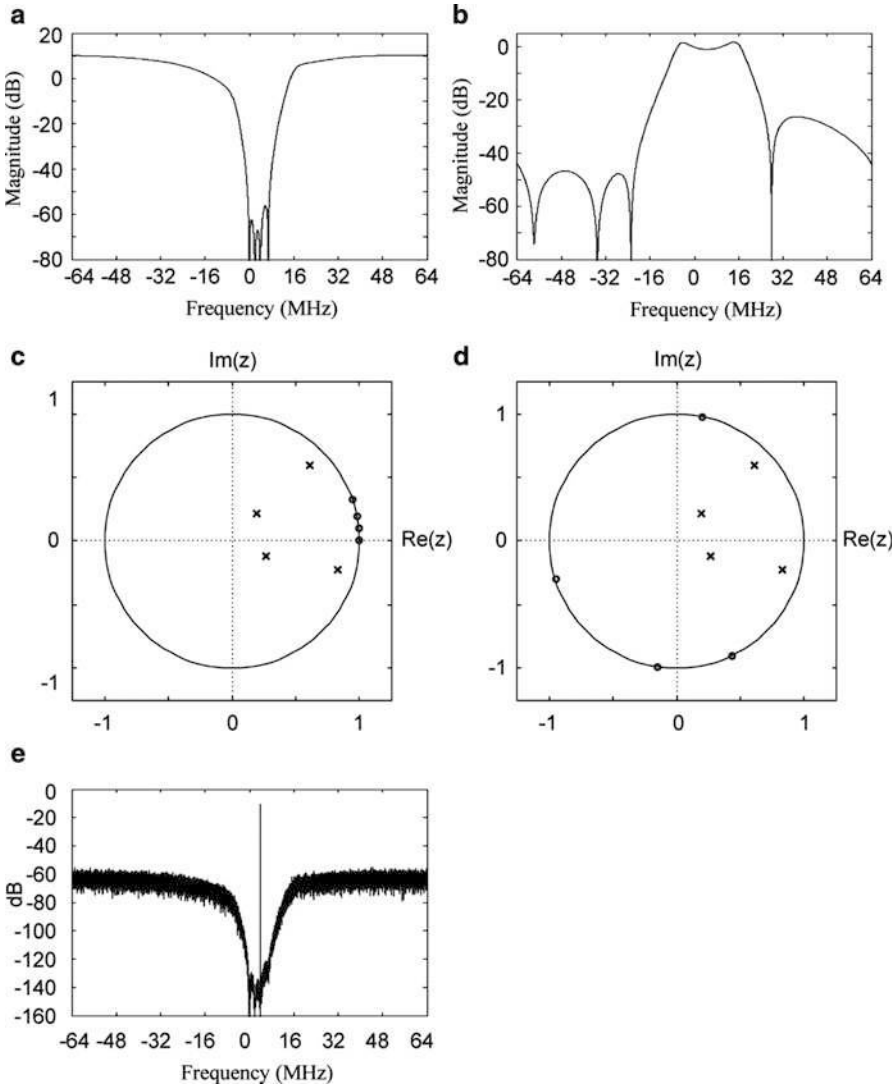


Fig. 3.26 Design of the STF-NTF using the optimization algorithm for $|L|_1 = 6.5$: (**a**) NTF magnitude gain, (**b**) STF magnitude gain, (**c**) NTF pole-zero plot, (**d**) STF pole-zero plot, (**e**) PSD plot of a complex ΔΣ modulator with STF and NTF transfer-functions as shown in (**a**) and (**b**)

designed for the same specifications using the algorithm proposed in Sect. 3.6. Figures 3.27–3.29 show the NTFs and the STFs generated using these two different approaches. A comparison of the two sets of STFs generated reveals that for the same value of SQNR, the optimization algorithm generates STFs with flatter passband, and an out-of-band rejection response which is at least superior by 7 dB (refer to Table 3.4).

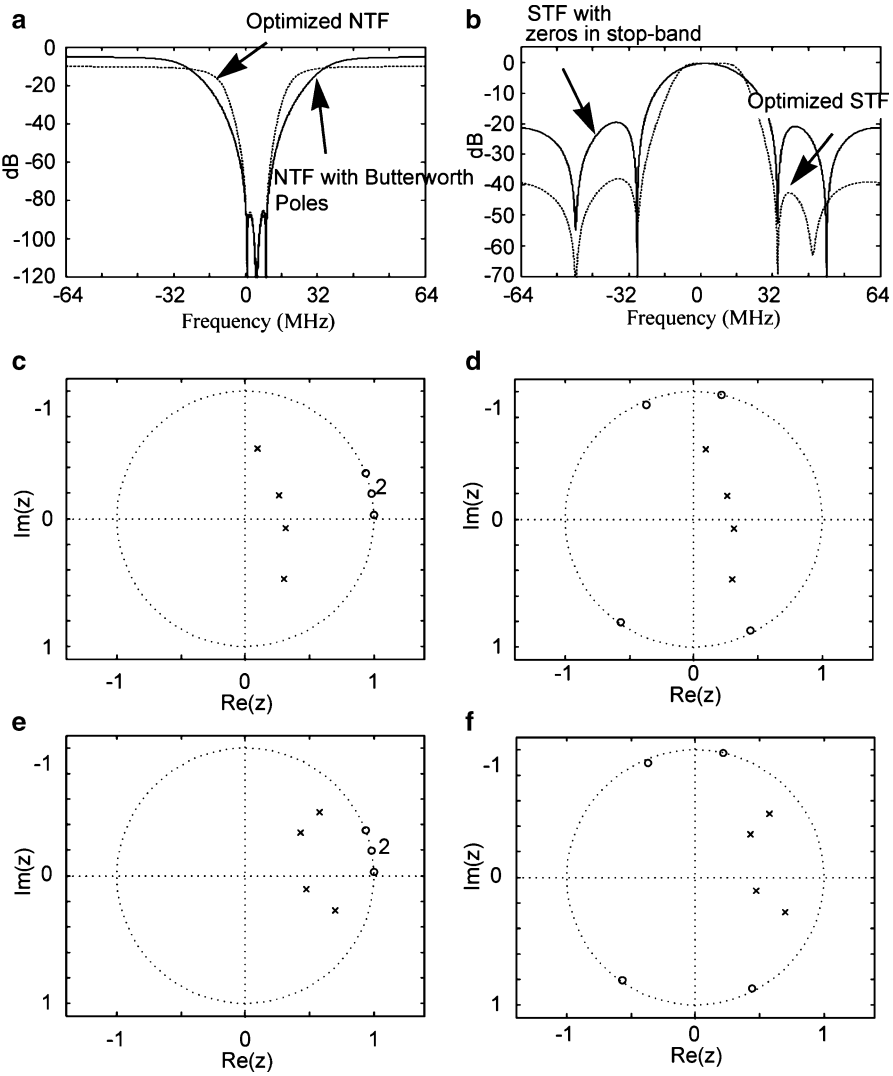


Fig. 3.27 Transfer functions for SQNR=101 dB. (**a**) NTF magnitude response, (**b**) pole-zero constellation for the non-optimized NTF, (**c**) pole-zero constellation for the optimized NTF, (**d**) STF magnitude response, (**e**) pole-zero constellation for the non-optimized STF, (**f**) pole-zero constellation for the optimized STF

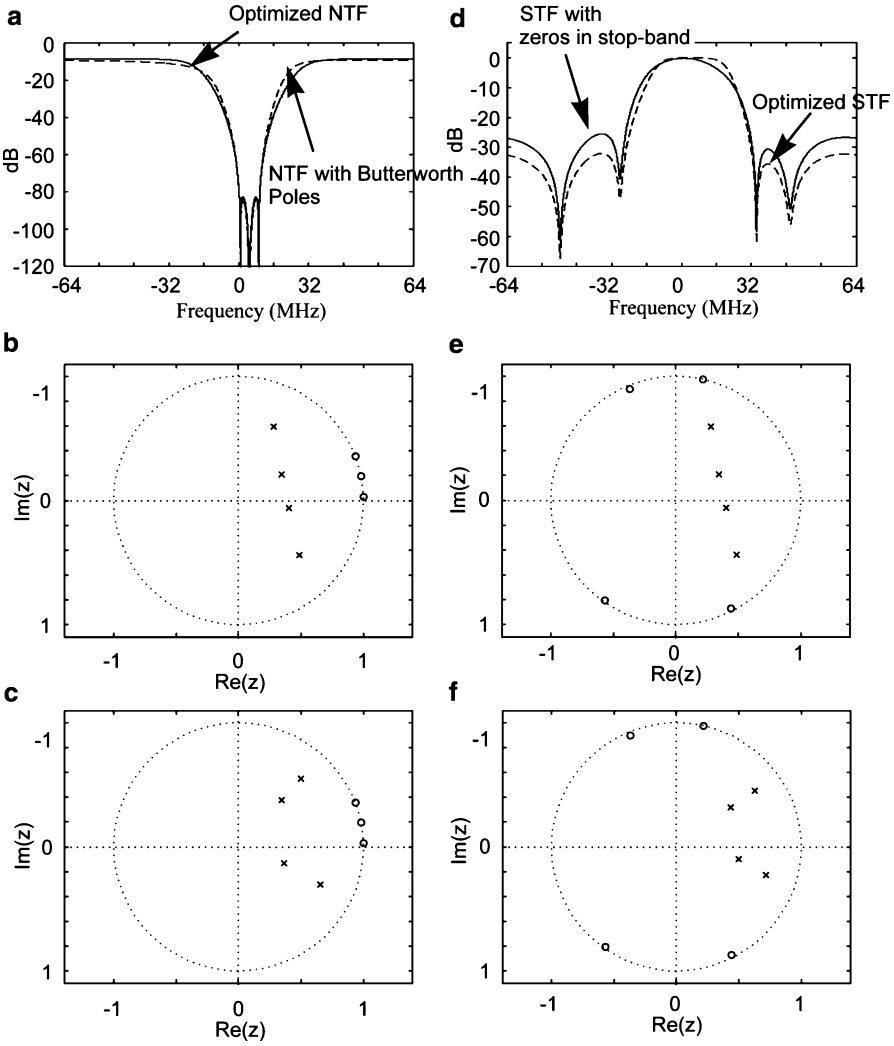


Fig. 3.28 Transfer functions for SQNR=94 dB. (**a**) NTF magnitude response, (**b**) pole-zero constellation for the non-optimized NTF, (**c**) pole-zero constellation for the optimized NTF, (**d**) STF magnitude response, (**e**) pole-zero constellation for the non-optimized STF, (**f**) pole-zero constellation for the optimized STF

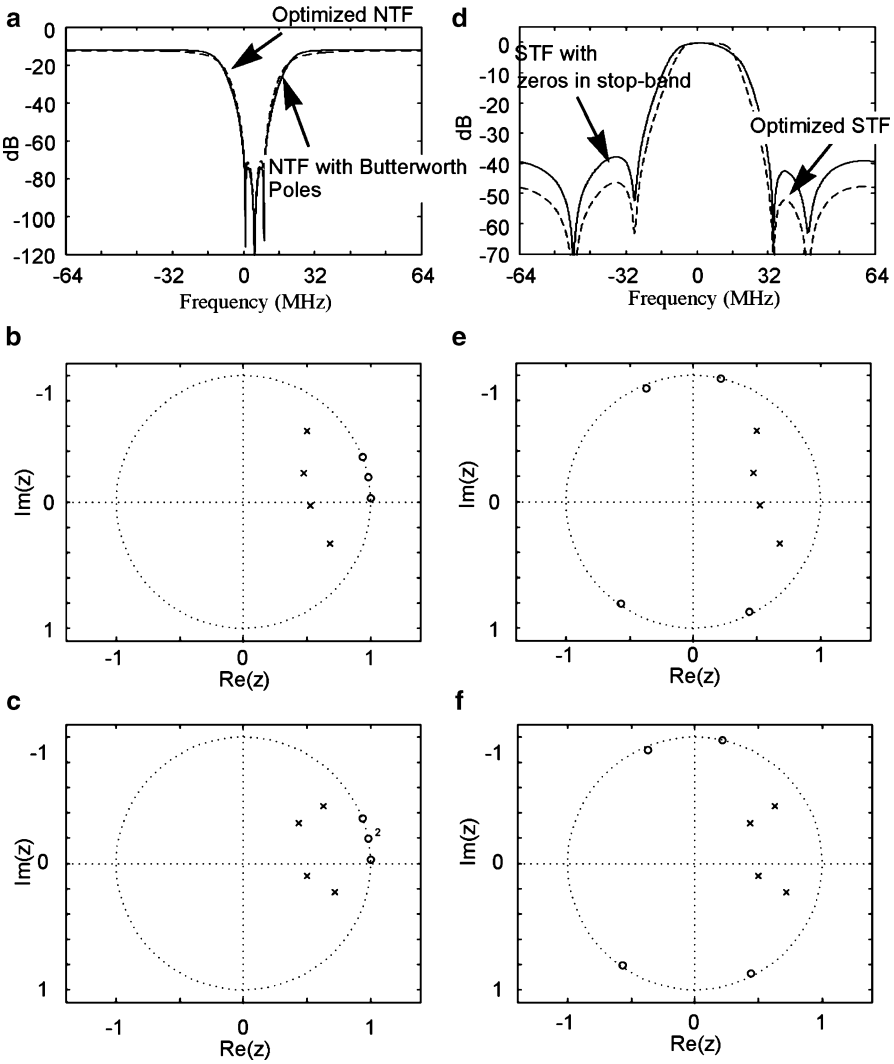


Fig. 3.29 Transfer functions for SQNR=89 dB. (**a**) NTF magnitude response, (**b**) pole-zero constellation for the non-optimized NTF, (**c**) pole-zero constellation for the optimized NTF, (**d**) STF magnitude response, (**e**) pole-zero constellation for the non-optimized STF, (**f**) pole-zero constellation for the optimized STF

Table 3.4 SQNR vs. stop-band attenuation performance summary

Stop-band attenuation (dB)		
Optimized	Non-optimized	SQNR(dB)
40	20	101
32	25	94
47	37	89

3.7 Power and Performance Analysis of the Proposed Complex ΔΣ Modulator

3.7.1 ΔΣ Modulator with Unity STF

Figure 3.30a shows a ΔΣ modulator topology where the input signal is fed directly to the quantizer [15]. The loop-filter of the modulator has been represented by the transfer function *H(z)*. As a result of the input to the quantizer the signal is directly fed to the quantizer without passing through the loop-filter of the modulator. As shown by (3.30) the magnitude of the STF of the modulator is unity across the frequency. The NTF of the modulator is same as that of any traditional ΔΣ modulator topology, Fig. 3.30b, with loop-filter *H(z)*.

$$\begin{aligned} STF(z) &= \frac{1}{1+H(z)} + \frac{H(z)}{1+H(z)} \\ &= 1 \end{aligned} \tag{3.30}$$

$$NTF(z) = \frac{H(z)}{1+H(z)} \tag{3.31}$$

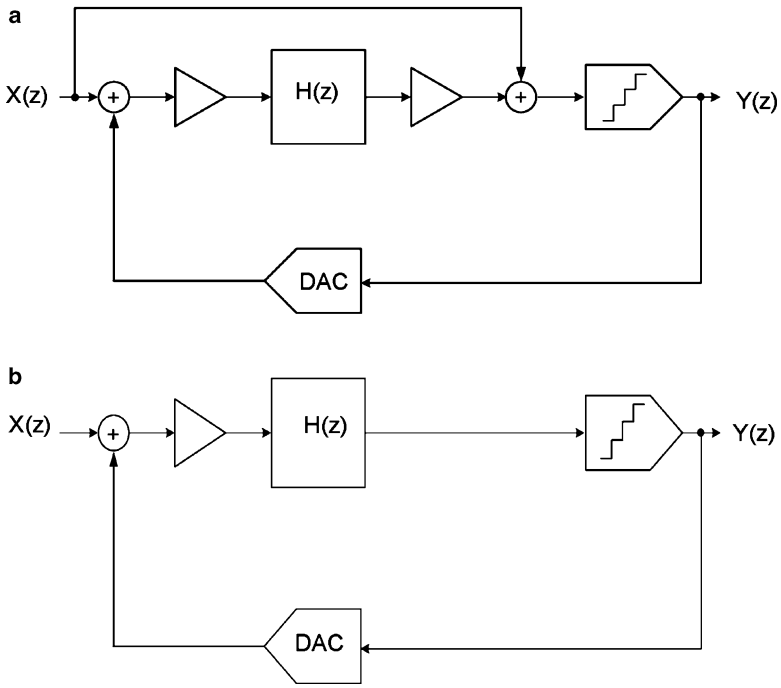


Fig. 3.30 (**a**) a ΔΣ modulator topology with a unity STF, (**b**) Traditional ΔΣ modulator topology

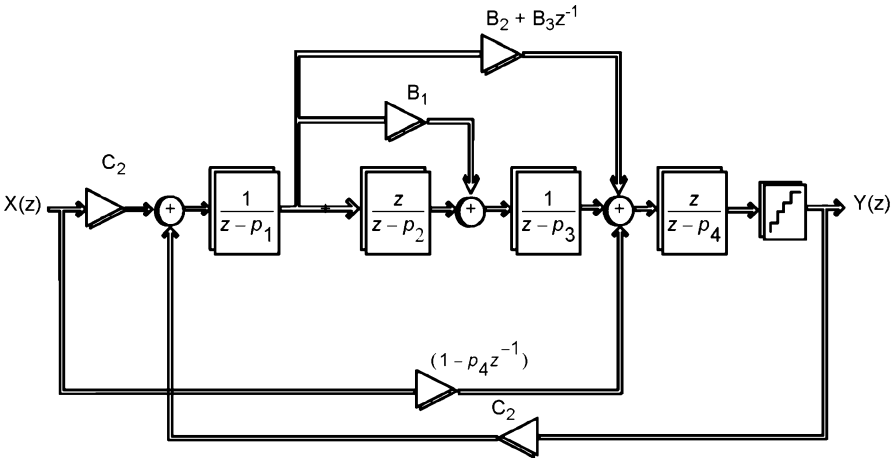


Fig. 3.31 Structure for a fourth-order ΔΣ modulator with a unity STF

An advantage of the ΔΣ modulator architecture shown in the Fig. 3.30a is that as the integrators are processing the quantization noise only the output swings of the opamps can be reduced with proper scaling of the coefficients. Depending on the choice of the coefficients, the linearity requirements of the opamps in the integrators maybe reduced and this results into an overall low-power consumption.

It is possible to transform the proposed modulator (refer to Fig. 3.2) into an unity STF modulator, refer to Fig. 3.31, by modifying the coefficients as shown in (3.32):

$$\begin{aligned} C_1 &= C_2 \\ F_1 &= 0 \\ F_2 &= 0 \\ F_3 &= -p_4 \\ F_4 &= 1 \end{aligned} \tag{3.32}$$

The proposed modulator with unity STF shown in the Fig. 3.31 avoids signal summation at the input of the quantizer by moving the signal feedforward to the input of the last integrator. A side-effect of signal feed-in at the last integrator input is that the integrator is processing both the signal and the quantization noise. However, due to the noise-shaping of the preceding stages of the modulator, the nonlinearities of the opamp in the last stage of the modulator have little impact on the SNDR of the modulator.

Despite the advantage of low-per consumption, feedforward ΔΣ modulators have some limitations that make them unsuitable for digitization of wireless signals. As discussed in Chap. 2, feedforward ΔΣ modulators require a front-end filter to compensate for the out-of-band peaking or slow roll off the STF [16]. The high-frequency interferers at the quantizer input can also react with the

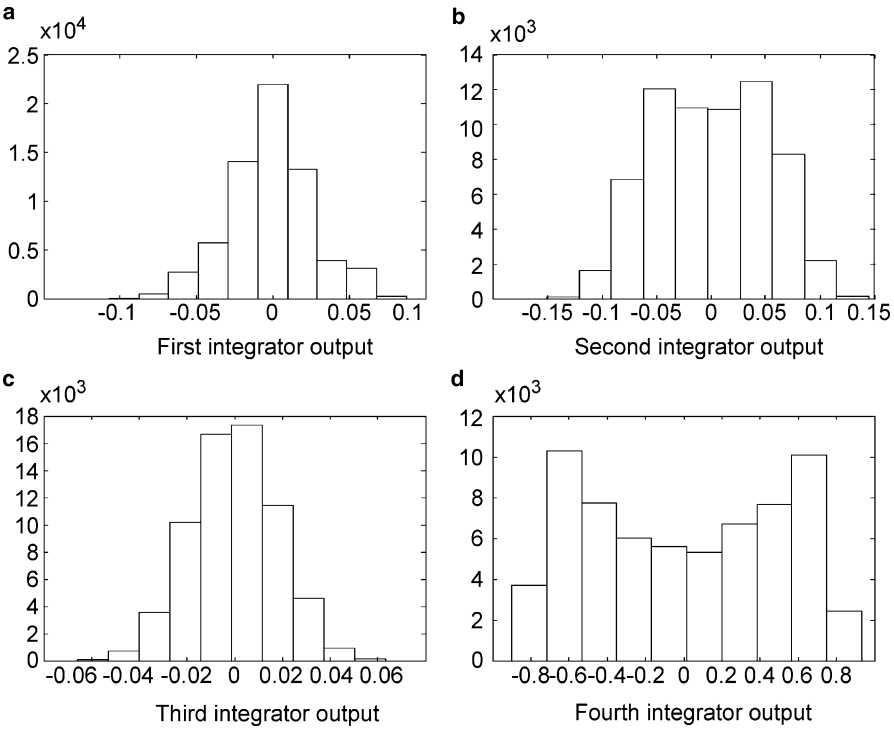


Fig. 3.32 Histogram plots of the integrator outputs for the feedforward modulator with unity STF

quantizer noise, which is large at these frequencies, and generate in-band intermodulation products, thus degrading the SNDR of the modulator [17].

In the following sub-sections the proposed ΔΣ modulator (referred to as FADC in further discussion), is compared to the feedforward ΔΣ modulator with unity STF. For reasons discussed in Chap. 4, the FADC has been modified by moving one of the zeros from the signal band to the image frequency. First, the power consumption of the two ADCs are compared. The next sub-section compares the impact of DAC and other coefficient mismatches on the two architectures. Finally, the FADC is compared with a Discrete-Time Receiver [18, 19].

3.7.2 Power Comparison

Figure 3.32 shows the signal swings at the integrator outputs for the feedforward modulator with unity STF, which are estimated through the use of a histogram plot from the behavioral model simulation in Matlab. Figure 3.33 shows the histogram plots of the integrator outputs for the proposed modulator with filtering STF.

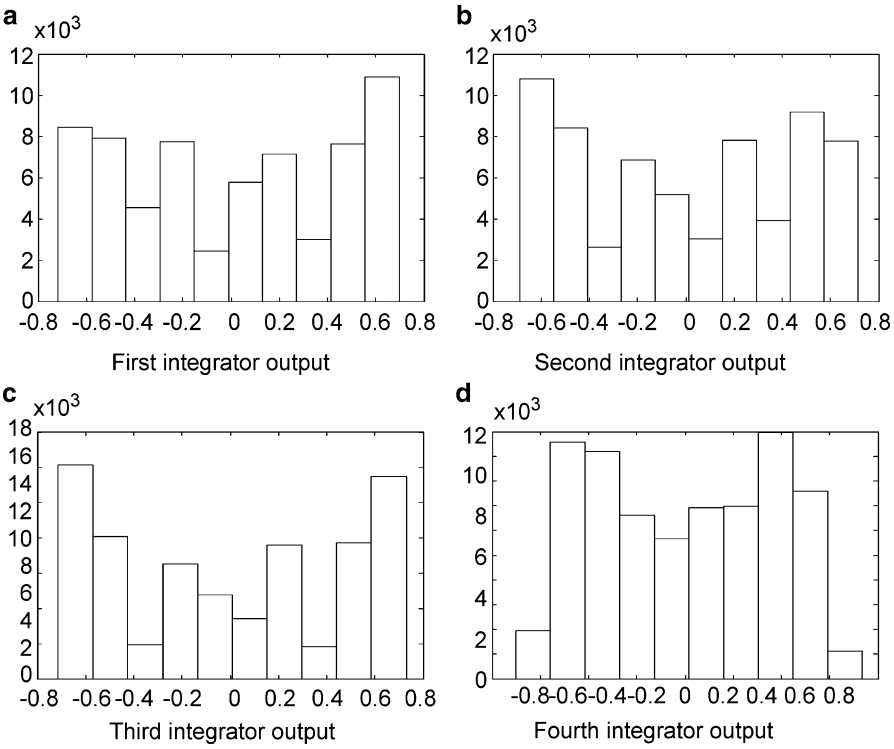


Fig. 3.33 Histogram plots of the integrator outputs for the modulator with filtering STF

A comparison between Figs. 3.32 and 3.33 reveals that the integrator swings for the modulator with unity STF are smaller; for example, for the first stage, the output swings are about one-sixth of the proposed FADC and have higher distribution around theoutput common-mode. This difference in integrator swings means that, assuming that the same sampling capacitor sizes are constrained by noise considerations, dynamic range scaling [8] can be applied to make the integrating capacitors smaller in the Σ ADC with unity STF. This application results in reduction of the area of the chip.

For the ΔΣADC with unity STF, the presence of unfiltered interfering signals, and hence large voltage steps from sample to sample at DAC input (refer to Fig. 3.34) translates into stringent settling requirements for the reference buffers driving the feedback DAC capacitors. These requirements mean that some of the power advantages of the ΔΣ ADC with unity STF may not be realized in actual implementation.

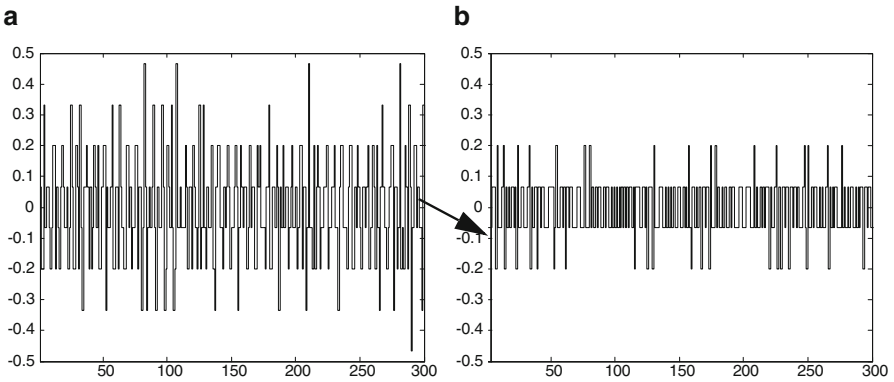


Fig. 3.34 DAC output swings for 300 samples for the triple tone test inputs: (**a**) feedforward ΔΣ modulator with unity STF, (**b**) proposed FADC

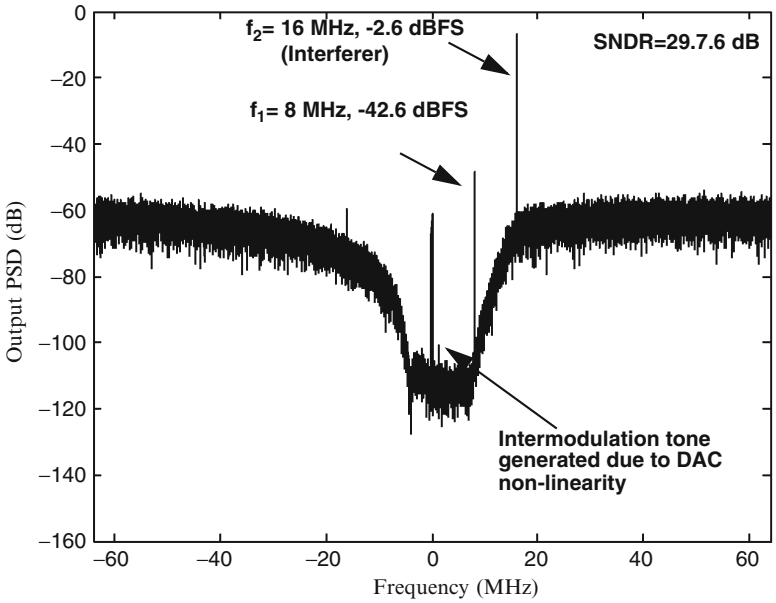


Fig. 3.35 PSD plot of the proposed complex ΔΣ modulator with a DAC mismatch = ±0.5% for a weak desired signal at −42.6 dBFS and a strong interferer at −2.6 dBFS

3.7.3 Sensitivity to Intermodulation Due to DAC Non-linearity

Figure 3.35 shows the output spectrum of the proposed ΔΣ modulator for a −42.6 dBFS input and a −2.6 dBFS interfering signal in the adjacent channel for a ±0.5% mismatch in the DAC elements.

To investigate the robustness of the proposed complex 4th order filtering ADC to intermodulation due to DAC mismatches, the proposed filtering ADC (FADC) was compared with the following ADCs:

- Complex 4th order Feedforward ADC with unity STF (referred to as FFADC in further discusssion),
- Complex 4th order Feedforward ADC with unity STF and an image zero (referred to as FFADC_IZ in further discusssion).

The ADCs were simulated in SIMULINK (Matlab) under the following conditions:

1. The discrete integrators have been modeled using αβγ representation [11]. The integrator model accounts for the finite dc gain and the output stauration voltages of the opamps.
2. The output saturation voltages of the integrators have been set at ±1.
3. Dynamic range scaling was performed to make the swings at the integrator outputs for the FFADC, FFADC_IZ, and FADC comparable.
4. A mismatch of ±0.5% was assumed for the DAC elements.

The input to the modulators is a triple-tone consisting of: (1) –46 dBFS input at 8 MHz, (2) two interfereres of strength –6 dBFS each at the frequencies of 20 MHz and 36 MHz respectively. This test pattern corresponds to the selectivity tests recommended for DVB-T compliant receivers [13]. For this test input the FFADC and FFADC_IZ show an SNDR of 43.5 dB and 32.3 dB respectively. The FADC achieves an SNDR of 32.5 dB for this test input. Figure 3.36 shows the swings at the integrator outputs for the FADC. As is evident from the figure, the integrators of the filtering ADC do not saturate for strong out-of-band interfering signals.

To determine the SNDR degradation of the modulators due to DAC mismatches, Monte Carlo simulations were run with a differential error 0.5% added to the DAC elements. Results from a set of 100 Monte Carlo simulations with a DAC mismatch of 0.5% show that the SNDRs of the FFADC and FFADC_IZ drop significantly and show an SNDR (95 percentile) of 14.6 dB and 15.2 dB respectively. The FADC shows comparatively lower degradation in the SNDR and shows an SNDR (95 percentile) of 23.5 dB (refer to Table 3.5) (Figs. 3.37–3.40)

Table 3.5 summarizes the comparison between the proposed modulator and the feedforward modulators with unity STF for the test input (–46 dBFS desired signal at 8 MHz, two interfering signals of strength –6 dBFS each and at the frequencies of 24 MHz and 36 MHz respectively).

For a reduced DAC mismatch of ±0.1% the SNDR (95th percentile) of the FADC degrades to 31.63 dB. For the FFADC and FFADC_IZ the SNDR degrades to 27.3 dB and 28.5 dB respectively.

3.7.4 Comparison with a Discrete-Time Receiver [18, 19]

A DTV receiver includes an IF filter and a demodulator for demodulation and error-correction of the IF signals. Currently, analog TV broadcasting and digital TV broadcasting are coexisting; hence, these interferences are mainly undesired

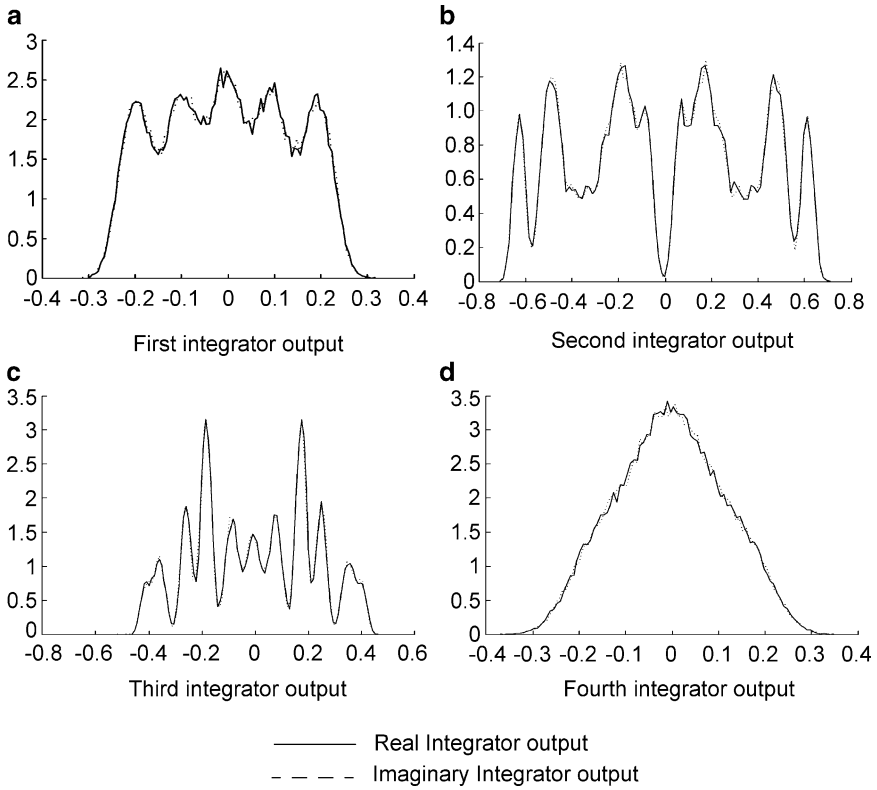


Fig. 3.36 Histogram plots of the integrator outputs for the modulator with filtering STF for the defined test input

Table 3.5 Simulated modulator performance with ±0.5% DAC mismatch

	SNDR (dB)	SNDR (95 percentile) (dB)
FFADC	43.5	14.6
FFADC_IZ	32.3	15.2
FADC	32.5	23.5

digital TV and/or analog TV channels. The power levels of those adjacent interfering channels can be higher than the desired channel, for example, 40 dB for ATSC signals [12]. In addition to the linearity requirement, it is necessary that the IF filters attenuate the interfering channels enough so that the ADC in the demodulator is not saturated. For example, for ATSC the IF filter has to provide over 50 dB attenuation for the adjacent channel.

The possible ways to implement IF filtering in a DTV receiver are:

Option 1- The IF filter is typically implemented using SAW filters and the receiver uses a bank of SAW filters to accomodate multi-standards. An advanatge

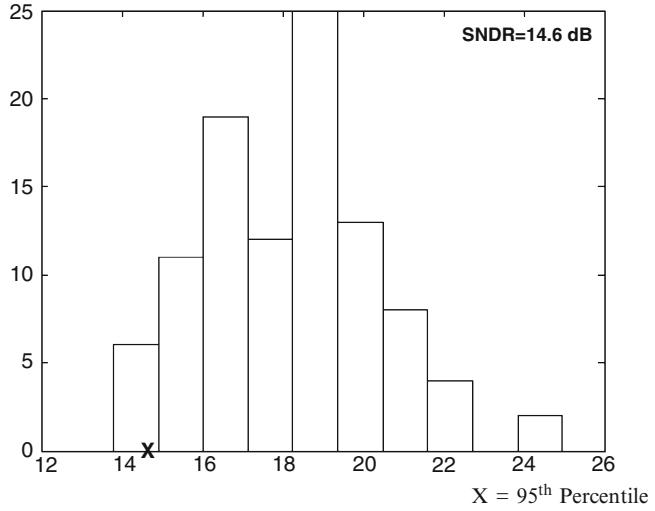


Fig. 3.37 Histogram plot of the SNDR for the feedforward modulator with unity STF for DAC mismatch = ±0.5%

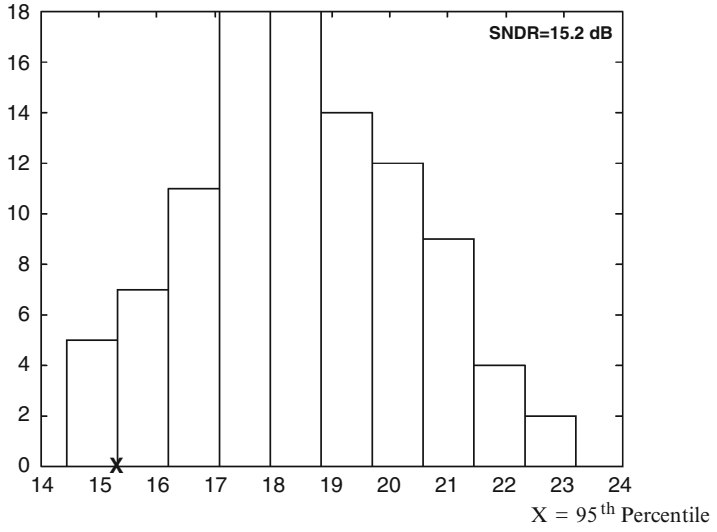


Fig. 3.38 Histogram plot of the SNDR for the feedforward modulator with unity STF with image zero for DAC mismatch = ±0.5%

of the SAW filters is the attenuation of the adjacent channels which results into a reduce dynamic range requiremenst of the ADC. However, to achieve a higher level of integration and hence low cost it is necessary to integrate the IF filters on the chip.

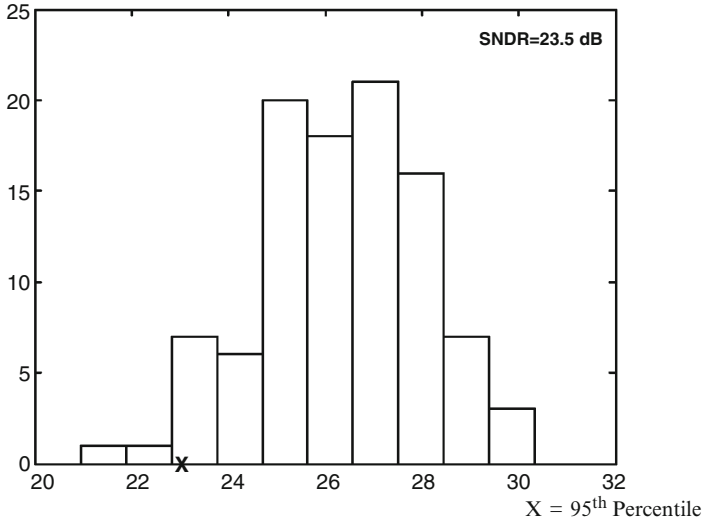


Fig. 3.39 Histogram plots of the SNDR for the filtering ADC for DAC mismatch = ±0.5%

Option 2- Two possible filter technologies for integrating IF filters on chip are: the continuous-time filters and the switched-capacitor filter. Though, the continuous-time filters consume less power, but they need calibration to set the frequency characteristics accurately. Also, the requirement to support multi-standards adds to the tuning complexity for these filters.

Unless, a narrow band IF filter is implemented for adjacent channel rejection, an ADC with greater than 11 bit resolution is required to digitize the adjacent interfering channel (refer to Table 3.6).

Option 3- A possible solution to reduce the dynamic range requirement of the ADC is the inclusion of a switched-capacitor (SC) filter to implement some of the channel filtering and selectivity at the input of the modulator (refer to Fig. 3.41).

Some of the advantages of implementing the filtering in the discrete-time domain, as compared with the continuous-time domain, are that SC filters do not require tuning to correct process and temperature-related variations, and also, because for SC filters frequency response depends only on the capacitor ratios and the clock frequency, these filters are easily amenable to multistandards. However, with SC filters, it is desirable to sample at a higher frequency to prevent the interfering signals aliasing into the signal-band. In addition, the quality of interfering signal suppression depends on the continuous-time anti-aliasing filter preceding the SC filter. The SC-filter can be followed by a decimation block for a sample-rate conversion to the analog-to-digital converter clock frequency. This sampling scheme can relax the requirements of the analog-to-digital converter, but at the cost of the order and complexity of the filters at the front-end. SC filters require opamps with greater bandwidth than the signal they are processing, and this requirement translates into

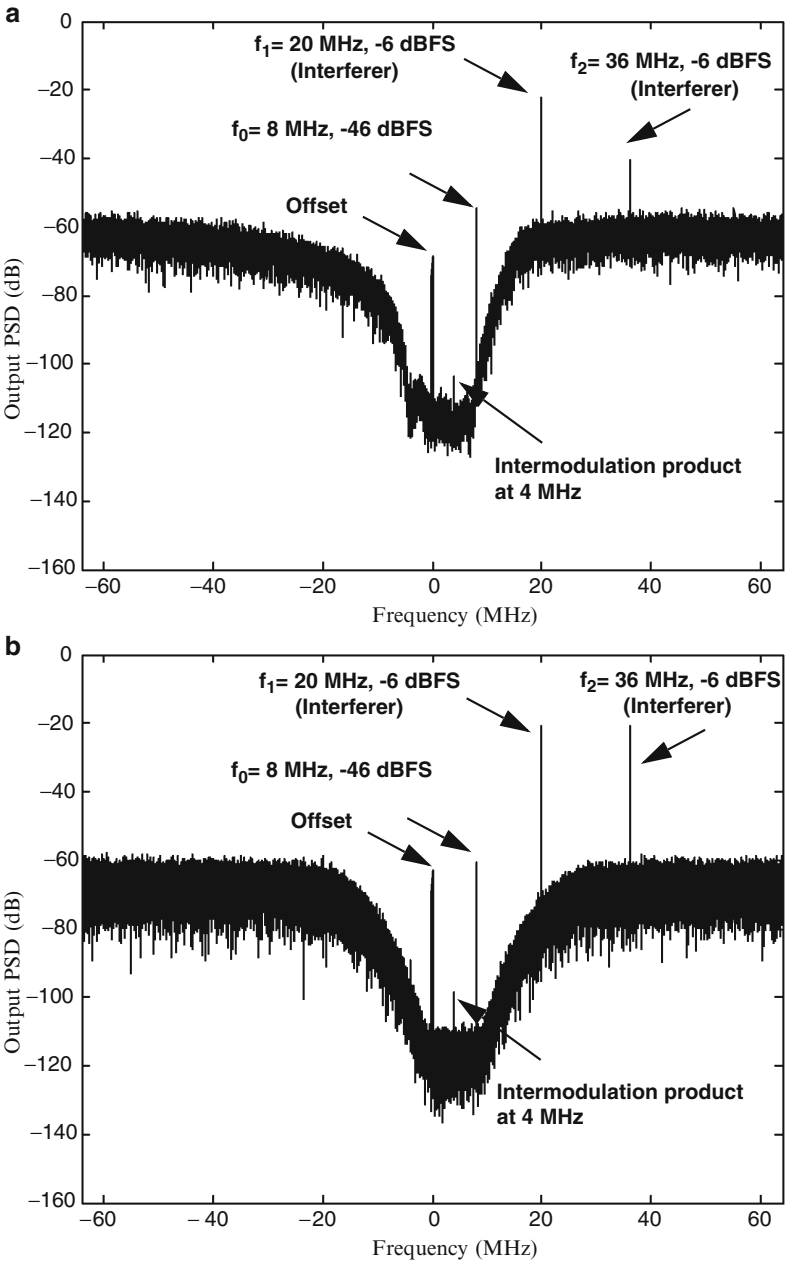


Fig. 3.40 PSD plots for the test input with a DAC mismatch of ±0.5% (**a**) proposed complex ΔΣ modulator, (**b**) feedforward complex ΔΣ modulator with unity STF

Table 3.6 Required number of ADC bits

Standard	C/N (dB)	Adjacent channel (dB)	ADC (No. of bits)
ATSC	15.5	40	10
DVB-T	27.5	35	11

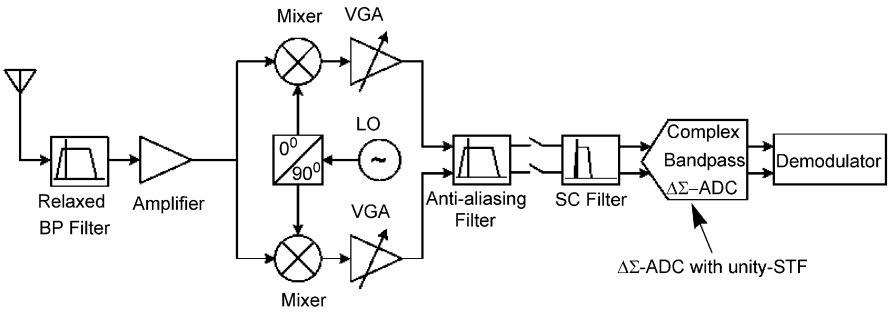


Fig. 3.41 A quadrature-IF system using a complex Low-IF ΔΣ modulator and a SC filter for channel filtering and selectivity

Table 3.7 Flexible SC filter and ADC architecture

SC filter order	Adjacent channel rejection (dB)	ADC (No. of bits)
–	–	12
3	10	10
4	20	9
8	60	6

higher power dissipation as compared to the continuous-time filters. Reduction of the switch thermal noise problem in SC filters may require large capacitors, and this requirement further compounds the power dissipation and bandwidth problems.

A trade-off exists between the attenuation characteristics of the IF filter and the dynamic range of the ADC. It is possible to find an optimum architecture by distributing the requirements between the filter and the ADC. Table 3.7 lists the possible SC filter order and the required ADC resolution to meet the requirements of the ATSC and DVB-T standards.

The first row in the table corresponds to the case where an ADC without a front-end SC filter is used for the digitization of the signal and the interferers. Considering the fact that high dynamic range ΔΣ modulators can be designed easily without the need for highly linear components, the first option in the table is advantageous over the other possible architectures in the table.

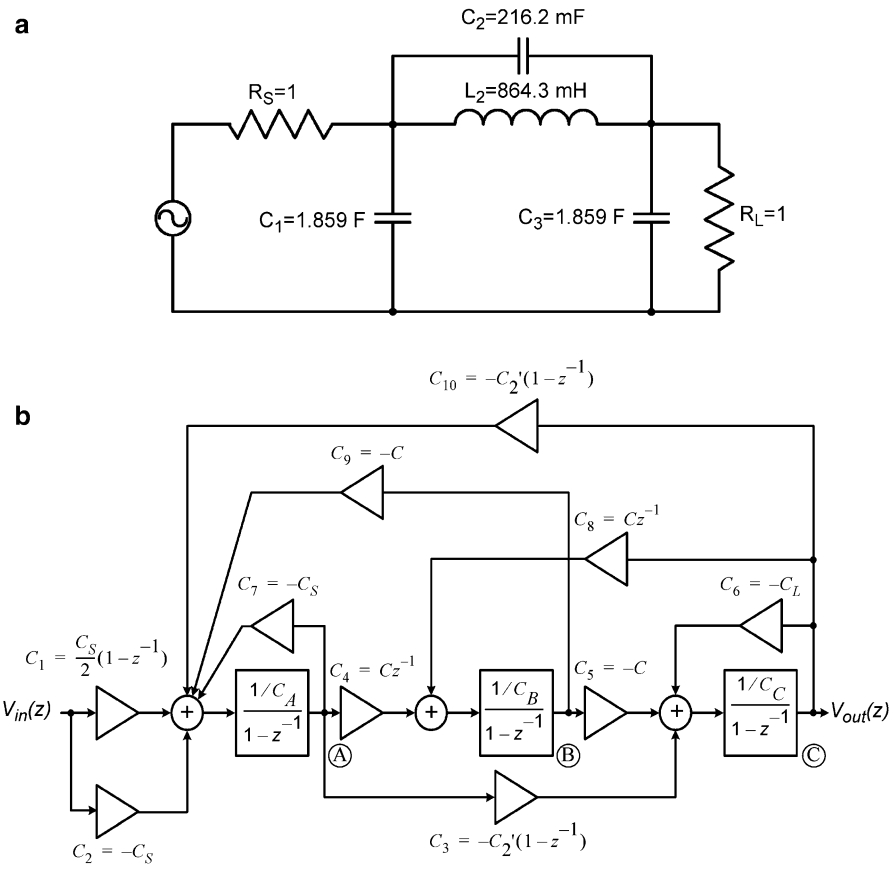


Fig. 3.42 (**a**) A third-order analog elliptic lowpass filter, and (**b**) SC lowpass filter

3.7.5 Comparison with an SC + FeedForward ADC with Unity STF

Alternatively, it is possible to use a feedforward ADC with unity STF and a relaxed SC filter at the front-end. The SC filter at the front-end attenuates the interferers and thus lowers the linearity requirements of the feedforward ΔΣ modulator. This section compares the power and performance of the proposed ΔΣ modulator with the architetcure comprising a feedforward ADC with unity STF and a relaxed SC filter at the front-end.

Figure 3.42a shows a third-order elliptic lowpass filter designed with following characteristics:

- stop-band attenuation = 40 dB,
- cut-off frequency = 1 radian/s,
- passband ripple = 0.2 dB.

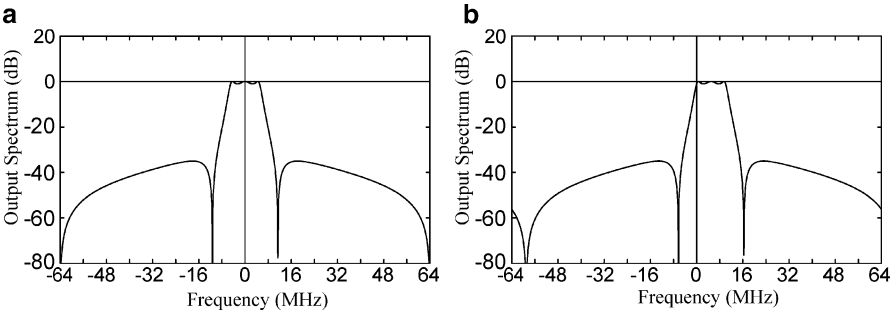


Fig. 3.43 Frequency-response of the third-order switched capacitor filter: (**a**) the real filter, and (**b**) the complex filter response

Following the procedure for the exact design of SC ladder filters described in [20] the analog filter was transformed into a switched-capacitor filter with following characteristics:

- stop-band attenuation A= 40 dB,
- sampling frequency f_s= 128 MHz,
- cut-off frequency f_c= 5 MHz.

Figure 3.42b shows the corresponding switched capacitor filter signal-flow graph. Compared to a third-order switched capacitor filter developed by cascading a first and second-order filter section, the filter shown has less sensitivity to element-value variations. Figure 3.43a shows the frequency response of the real switched capacitor filter. The notches at (f_s/2) are due to the zeros introduced by the bilinear transformation.

Figure 3.43b shows the response of the complex filter obtained by frequency shifting the variable z in the transfer function:

$$z \rightarrow ze^{-j\omega_o T} \tag{3.33}$$

where ω_o is the frequency shift, and T (=1/f_s) is the sampling period.

Table 3.8 list the capacitor sizes for the real switched capacitor filter. The 'scaled values' column lists the capacitor sizes scaled for maximum dynamic range for each amplifier.

The frequency responses of the three amplifier outputs of the switched-capacitor filter for the scaled capacitor values are shown in Fig. 3.44.

Interesting information can be obtained by plotting the transfer functions from the integrator outputs to the filter output. The transfer function from the last integrator output to V_{out}, $V_{out,C}$, reveals the poor quality of the NTF for a ΔΣ modulator designed with this switched-capacitor filter as the loop-transfer function. The other two transfer-functions represent the contribution of noise-sources at each integrator stage input to the switched-capacitor output voltage V_{out} ; for example,

Table 3.8 Component values for the switched-capacitor filter

Component	Unscaled values	Scaled values for dynamic range	Scaled values for SNR (pF)
C_1	0.1233	0.2467	0.1
C_2	0.2467	0.4935	0.2
C_3	−0.2338	−0.2338	−0.070
C_4	1	3	0.1
C_5	−1	−0.3333	0.1
C_6	0.2467	−0.3333	0.1
C_7	−0.2467	−0.2467	−0.1
C_8	1	3	0.1
C_9	−1	−0.3333	−0.135
C_{10}	−0.2338	−0.2338	−0.094
C_A	1.9695	1.9695	0.7965
C_B	14.2039	14.2039	0.473
C_C	1,9695	14.2039	4.2

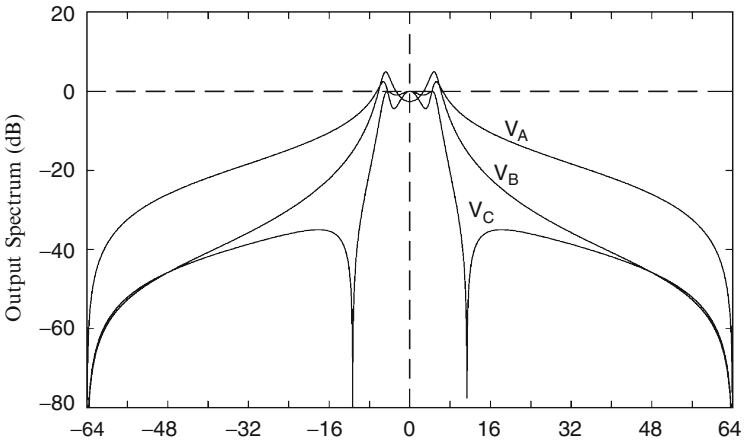


Fig. 3.44 Amplifier output voltages response of the third-order switched capacitor filter

$V_{\text{out,A}}$, $V_{\text{out,B}}$ represent the noise contributions of the sampling switches connected to the capacitors C_4 and to C_5 respectively to the output of the filter. These transfer-functions reveal the absence of noise-shaping found in a ΔΣ modulator; this absence of noise-shaping is related in a way to the trade-off involved between the quality of the STF and the NTF in a ΔΣ modulator. The absence of noise-shaping (Fig. 3.45) means that each stage of the filter has to be designed for minimum switch and opamp noise and other circuit nonlinearities.

Table 3.8, which does not take the amplifier noise into account, lists the capacitor values required to achieve a signal-to-thermal-noise ratio of 80 dB at an oversampling-ratio of 16 at the output of the switched-capacitor filter [21] (refer to Chap. 4). A comparison of these capacitor values and the values derived for the proposed ΔΣ modulator shows that each of the filter stages can be expected to have power consumption similar to the first-stage of the proposed ΔΣ modulator.

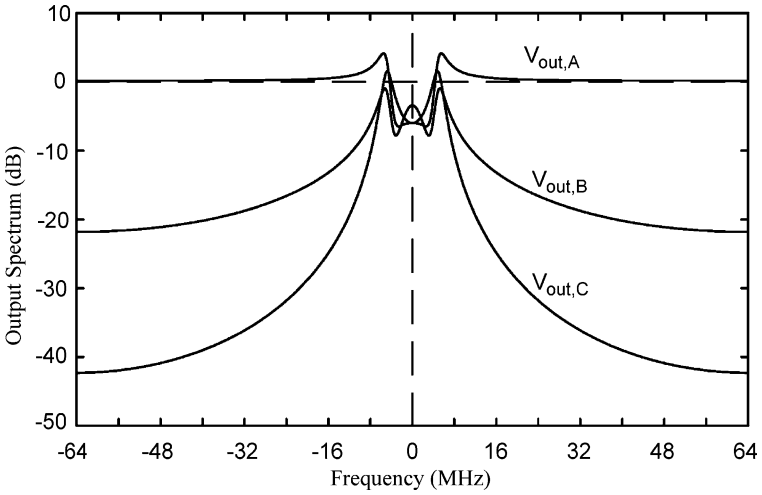


Fig. 3.45 Frequency response of the noise transfer functions of the third-order switched capacitor filter

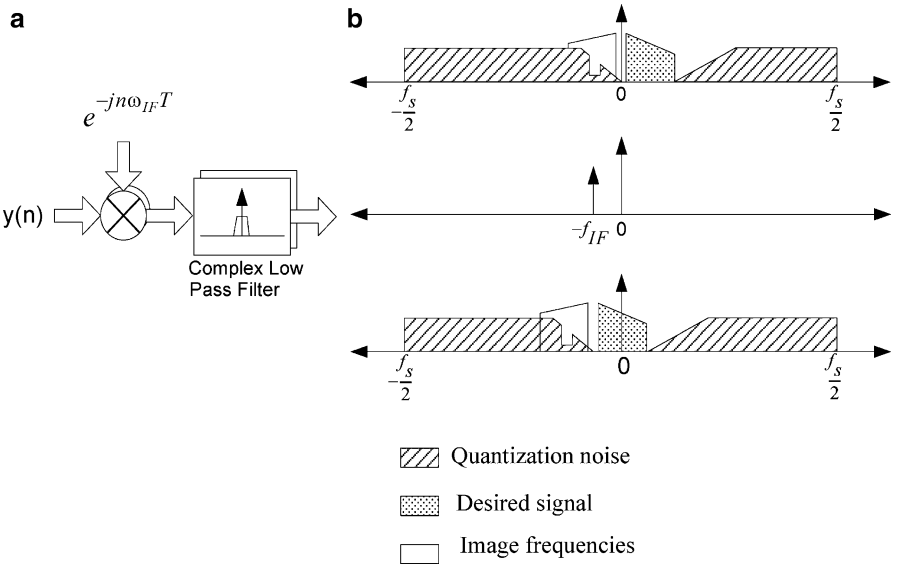


Fig. 3.46 (**a**) A complex mixer for decimation of output bit-stream of complex ΔΣ modulator. (**b**) Frequency domain illustration of complex decimation

It is possible to convert the real switched capacitor filter into a complex switched capacitor filter by replacing each element of the real filter with a corresponding frequency-shifted complex element. A complex filter derived from a dynamic range scaled lowpass filter preserves the optimum dynamic range of the low-pass filter [22].

For a real SC filter, component variations change the location of the poles and zero, whereas, for a complex filter mismatches can completely alter the complex filter transfer function and significantly degrade the SNR of the filter [14]. Study of the sensitivity of complex filters to component mismatches has been done in [23] and [24]. It has been observed that the component mismatches of the final stage of the complex SC filter have a greater effect on the stop-band response, and the final stage of the complex SC filter should be designed with large and carefully matched devices. This is unlike a ΔΣ modulator, in which the first integrator stage amplifier is typically dominant in the modulator noise, linearity, and power requirements.

The conclusion is that, due to the reduced power and linearity requirements of the amplifier, feedforward ΔΣ modulator with unity STF is an attractive option, however this receiver architecture results into an increased complexity of the filter at the front-end. The noise and matching requirements of these front-end filters outweigh the advantages gained from the feeforward ΔΣ modulator architecture.

3.8 Decimation for Complex ΔΣ Modulators

The output of the complex ΔΣ modulator is at the intermediate frequency, f_{IF}, and a complex decimator is required to reduce the bit rate of the modulator. The complex bitstream is modulated to baseband by mixing with $e^{-jn\omega_{IF}T}$ ($T = 1/F_s$, where F_s is the sampling frequency) and then filtered by a complex low-pass filter (Fig. 3.46). Modulating complex bit-stream to DC requires multiplying of two complex numbers, however, a suitable choice for f_{IF} frequency simplifies the architecture for the mixer and the complex filter. For example, for $\omega_{IF}T = \pi/2$, $e^{-jn\omega_{IF}T}$ can be decomposed into a sum of $0, \pm 1$ streams multiplied by constants.

$$e^{-jn(\pi/2)} = (1,\ 0,\ -1,\ 0,\ \ldots) + j(0,\ -1,\ 0,\ 1,\ \ldots)$$

For this choice of the IF frequency, demodulation can be simplified as shown Fig. 3.47:

3.9 Advantages of the Proposed ΔΣ Modulator Architecture

The proposed ΔΣ modulator offers several advantages over the traditional ΔΣ modulator architectures:

- Unlike the feedforward architecture, the proposed ΔΣ modulator avoids having a weighted summation before the quantizer, and, hence, issues like signal attenuation and reference scaling for the purpose of passive summation or power dissipation in the case of active summation have been eliminated. In the proposed ΔΣ modulator, the summation of the signals has been distributed at various integrator inputs.

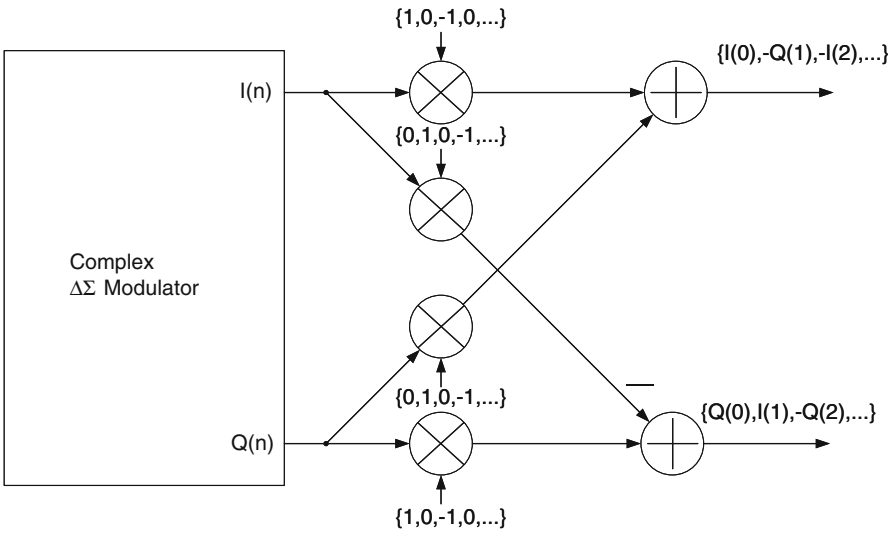


Fig. 3.47 Complex demodulation of the complex ΔΣ modulator output

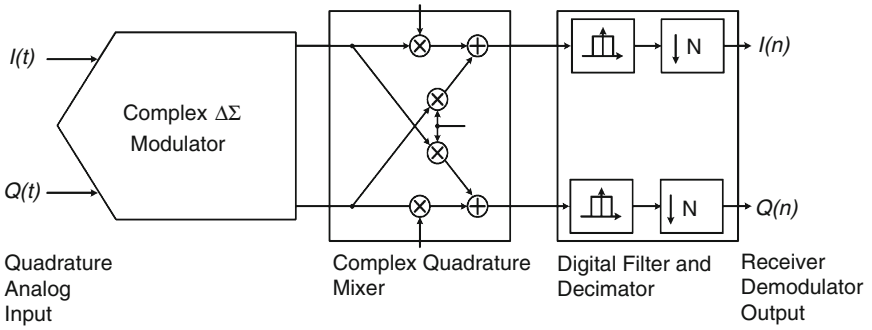


Fig. 3.48 Architecture for a DTV receiver demodulator

- Due to the low-pass nature of the STF, the modulator avoids stability issues related to the peaking of the STF at higher signal frequencies. Compared to the traditional feedforward ΔΣ modulator, the proposed modulator shows significantly reduced sensitivity to process variations and coefficient mismatches. This reduction occurs because of the filtering nature of the STF.
- With a filtering STF and stop band attenuation greater than 30 dB, the ΔΣ modulator reduces intermodulation of the desired signal and the interfering signals at the input of the quantizer, and also avoids feedback of the high-frequency interfering signals at the input of the modulator.
- Figure 3.48 shows digital signal processing in a typical ΔΣ modulator-based DTV receiver. The task of the complex demodulator includes demodulation and recovery of the transmitted bit sequence. Prior to lowering the bit-rate,

the decimation filters at the output of the complex bandpass ΔΣ ADC attenuate the high-frequency quantization noise and out-of-band interferers components that may alias into the signal band during decimation. The order of the decimating filters is decided by the required attenuation of the quantization noise and the interfering signals at the input of the decimating filters. The interfering signals are attenuated by the antialias filter at the input of the ADC. The filtering STF of the ADC further relaxes the decimation filter design by attenuating these interferers.

- The role of the digital quadrature mixer, the complex NCO in Fig. 3.48, consists of correcting any frequency offset errors that may occur between the carrier frequency and the symbol rate and converting the complex signal from low-IF to zero-IF. The baseband signal at the output of the mixer is subsequently low-pass filtered in order to attenuate image frequencies and other sum frequencies generated by the mixing operation. The output of the low-pass filters goes to a data recovery block where the transmitted data bit sequence is recovered. The low-pass filters act as image rejection filters, and the order of these low-pass filters depends on the attenuation desired for the image frequencies. An asymmetric filtering ADC with significant attenuation for image frequencies reduces the complexity of these low-pass filters.

References

1. K. Martin,"Approximation of Complex IIR Bandpass Filters Without Arithmetic Symmetry," *IEEE Trans. Circuits and Systems-I*, vol. 52, No. 4, pp. 794–803, April 2005.
2. S. R. Norsworthy, R. Schreier, and G. C. Temes, Eds., *Delta-Sigma Data Converters: Theory, Design, and Simulation*. New York: IEEE Press, 1997. ISBN 0780310454.
3. Richard W. Daniels, *Approximation Methods for Electronic Filter Design: With Applications to Passive, Active, and Digital Networks*, McGraw-Hill, 1974.
4. Peter O. Brackett, A.S.Sedra, *Filter Theory and Design: Active and Passive*, Matrix Series in Circuits and Systems.
5. Bupesh Pandita, K. W. Martin, "Designing Complex Delta Sigma Modulators with Signal-Transfer Functions having Good Stop-Band Attenuation," pp. 3626–3629, ISCAS 2007.
6. Richard Schreier and Gabor C. Temes, *Understanding Delta-Sigma Data Converters*. Wiley-IEEE Press, 2004. ISBN 0-471-46585-2.
7. KiYoung Nam, Sang-Min Lee, D. K. Su, and B. A. Wooley, "A low-voltage lowpower sigma-delta modulator for broadband analog-to-digital conversion," *IEEE J. Solid-State Circuits*, vol. 40, no. 9, pp. 1855–1864, Sep. 2005.
8. Richard Schreier, "An Empirical Study of High-Order Single-Bit Delta-Sigma Modulators," *IEEE Transactions on circuits and systems-II: analog and digital signal processing*, vol. 40, no. 8, August 1993.
9. John. G. Kenney, and L. Richard Carley, "Design of multibit noiseshapingdata converters," *Analog Integrated Circuits and Signal Processing*, vol. 3, no. 3, May 1993.
10. The Math Works, Inc., *Matlab*, Version 6.4, Natick, Massachusets: The Math Works, Inc., R14, 2005.
11. *ATSC Recommended Practice: Receiver Performance Guidelines*, ATSC A/74, June 2004, pp 13–14.

12. *Mobile and Portable DVB-T/H Radio Access Interface Specification*, EICTA MBRAI-02, Jan 2004.
13. S.A. Jantzi, K. W. Martin, and A. S. Sedra, "The effects of mismatch in complex bandpass ΔΣ modulators," *IEEE International Symposium on Circuits and Systems*, vol. 1, 12–15, May 1996, pp. 227–23.
14. R. B. Staszewski, K. Muhammad, D. Leipold, Chih-Ming Hung, Yo-Chuol Ho, J. L. Wallberg, C. Fernando, K. Maggio, R. Staszewski, T. Jung, Jinseok Koh, S. John, Irene Yuanying Deng, V. Sarda, O. Moreira-Tamayo, V. Mayega, R. Katz, O. Friedman, O. E. Eliezer, E. de-Obaldia, P. T. Balsara, "All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS," *IEEE Journal of Solid-State Circuits*, Volume 39, Issue 12, pp 2278–2291, December 2004.
15. Zhiyu Ru, E. A. M. Klumperink, B. Nauta, "On the Suitability of Discrete-Time Receivers for Software-Defined Radio," *IEEE International Symposium on Circuits and Systems*, 2007, 27–30 pp. 2522–2525, May 2007.
16. W.-H. Ki, G. C. Temes, "Low-phase-error offset-compensated switched-capacitor integrator," *Electronics Letters*, Volume 26, Issue 13, 21 June 1990, pp.957–959.
17. Anas A. Hamoui, *Delta-Sigma Data Converters for Broadband Digital Communications*, Ph.D. Thesis, University of Toronto, 2004.
18. J. Silva, U. Moon, J. Steensgaard, G. C. Temes, "Wideband low-distortion deltasigma ADC topology," *Electronics Letters* Volume 37, Issue 12, 7 June 2001 pp 737–738.
19. E. H. Dagher, P. A. Stubberud, W. K. Masenten, M. Conta, T. V. Dinh, "A 2-GHz analog-to-digital delta-sigma modulator for CDMA receivers with 79-dB signal-tonoise ratio in 1.23-MHz bandwidth," *IEEE J. Solid-State Circuits*, vol. 39, pp. 1819–1828, November 2004.
20. K. Philips, P. A. C. M. Nuijten, R. L. J. Roovers, A. H. M. van Roermund, F. M. Chavero, M. T. Pallares, A. Torralba, "A continuous-time ΣΔ ADC with increased immunity to interferers," *IEEE J. Solid-State Circuits*, vol. 39, issue. 12, pp. 2170–2178, December 2004.
21. Roubik Gregorian, Gabor C Temes, *Analog Mos Integrated Circuits for Signal Processing*, Wiley Series On Filters, Wiley-Interscience, 1986.
22. R. Schreier, J. Silva, J. Steensgaard and G.C. Temes, "Design-oriented estimation of thermal noise in switched-capacitor circuits," *IEEE Transactions on Circuits and Systems*, vol. 15, no. 11, pp. 2358–2368, November 2005.
23. Q. L. Liu, W. M. Snelgrove, and A.S. Sedra, "Switched-capacitor implementation of complex filters," *Proceedings of the 1986 IEEE ISCAS*, vol. 3, pp. 1121–1124, May 1986.
24. A. S. Sedra, W. M. Snelgrove, and R. Allen, "Complex analog bandpass filters designed by linearly shifting real low-pass prototypes," *Proceedings of the 1985 IEEE ISCAS*, vol. 3, pp. 1223–1226, June 1985.
25. R. H. Allen, "Complex analog filters obtained from shifted lowpass prototypes", M.A.Sc. thesis, University of Toronto, 1985.

Chapter 4
Architectural-Level Design of the Experimental ΔΣ Modulator

This chapter provides background information for "image transfer function" related to mismatches in complex filters. The impact of mismatches on the modulator proposed in Chap. 3 is examined, and on the basis of the results, an improved complex ΔΣ modulator is proposed.

The chapter further discusses the architectural-level design of the proposed complex ΔΣ modulator. The SC circuit configuration for the realization of a nondelaying complex integrator, clocking, the number of quantization bits, and the dynamic-range scaling are discussed. The SC implementation nonidealities like noise, finite resistance of the switches, finite dc gains of the opamp, etc., are considered in order to arrive at the SC circuit specifications for a complex ΔΣ modulator with a SNR of 75 dB over a signal bandwidth of 8 MHz, at a sampling frequency of 128 MHz. The chapter also presents behavioral simulation results for the experimental ΔΣ modulator.

4.1 Background

A complex ΔΣ modulator is realized with complex poles. Figure 4.1 describes the realization of a complex pole with two real integrators. As seen in the figure, the complex pole realization can be considered a two-input two-output real system, with the additional condition that the inputs and outputs are quadrature signals [1].

A mismatched complex filter can be represented with two complex filters. In Fig. 4.2a, the first ideal complex filter operates on the input signal, and the second, the *image transfer function*, operates on the input signal after conjugating it. The conjugation of the image frequency means the transfer of energy at the image frequency into the signalband and vice versa. This transfer of the image frequency into the signal-band, which defines image rejection of the complex filter, can degrade the quality of the signal at the output of the complex filter.

Figure 4.2b shows the ideal signal response and the image response of a complex filter with a pole of magnitude 0.9 at an angular frequency of $\pi/2$. The image

B. Pandita, *Oversampling A/D Converters with Improved Signal Transfer Functions*, Analog Circuits and Signal Processing, DOI 10.1007/978-1-4614-0275-6_4,

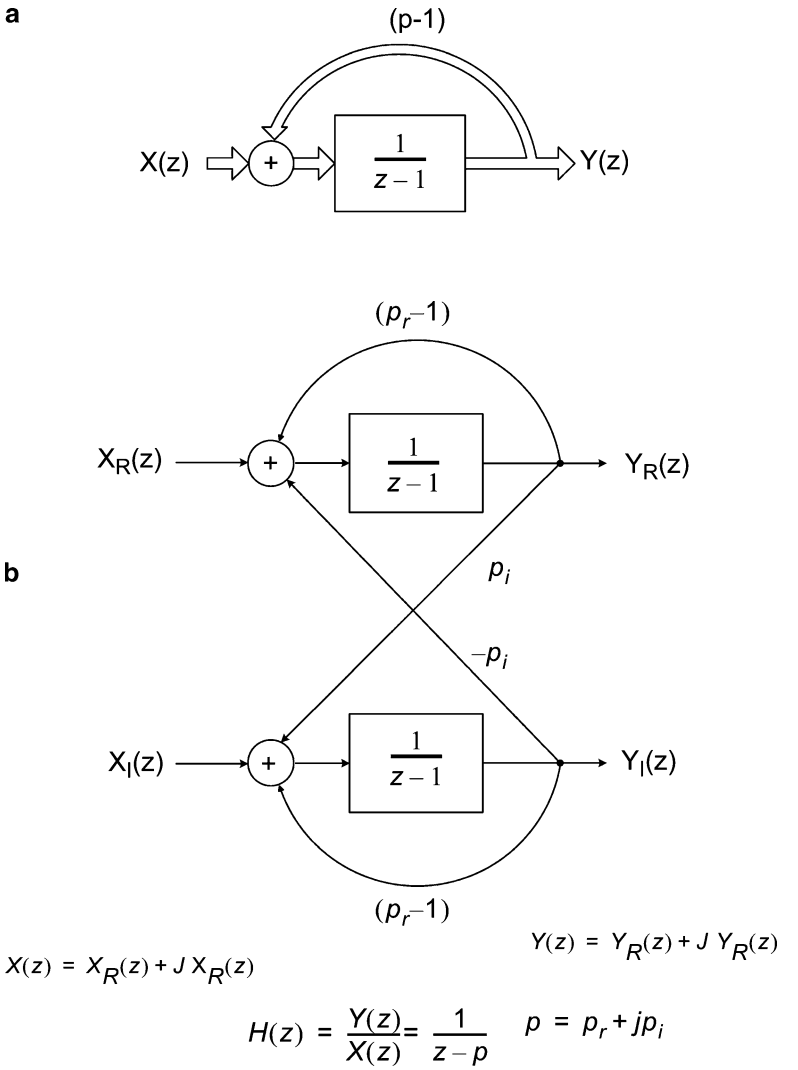


Fig. 4.1 Realizing a complex pole at $p = p_r + jp_i$ using (**a**) a complex signal flow graph and (**b**) a two-input two-output real linear signal flow graph

response was obtained by introducing a mismatch of $\pm 0.1\%$ in the complex filter coefficients, refer to Fig. 4.3. As can be seen from the image response plot, an input at the image frequency $\omega = -\pi/2$ has aliased into the output at $\pi/2$. In this example given, the signal response and the image response indicate that with a mismatch of $\pm 0.1\%$ the complex filter has an image rejection (IMR) of 63.07 dB at the signal frequency of $\pi/2$. The example underlines the significance of component matching in a complex system.

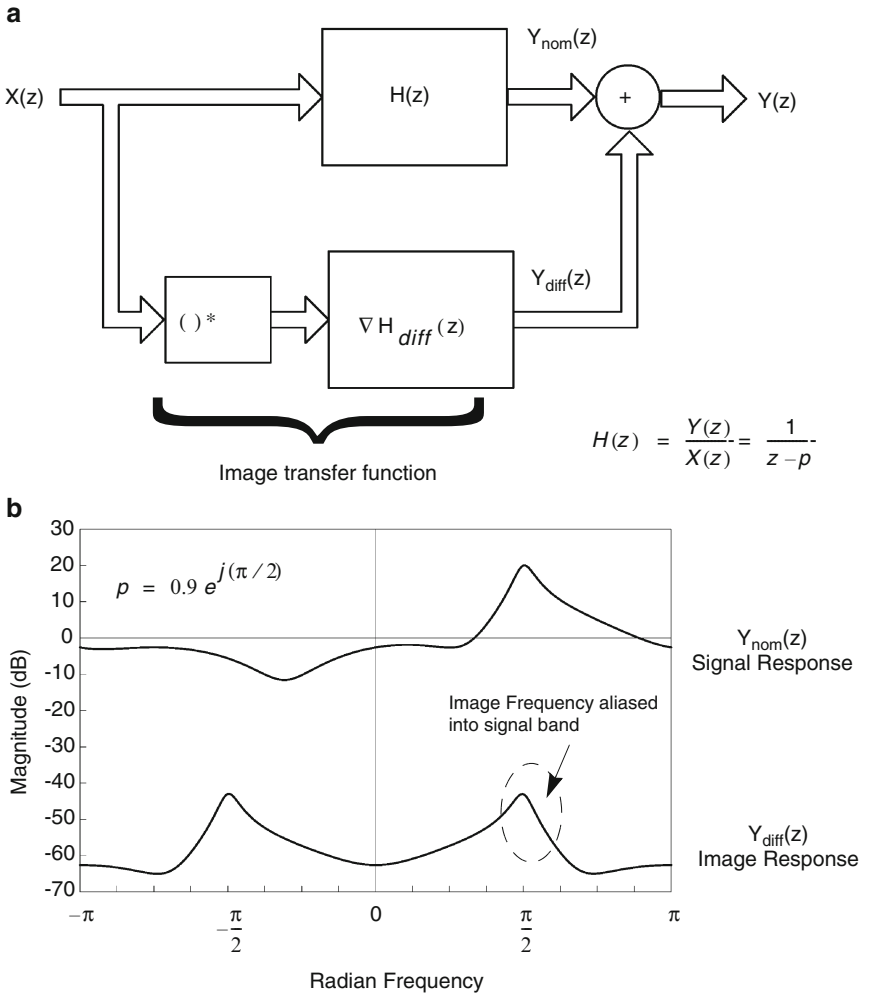
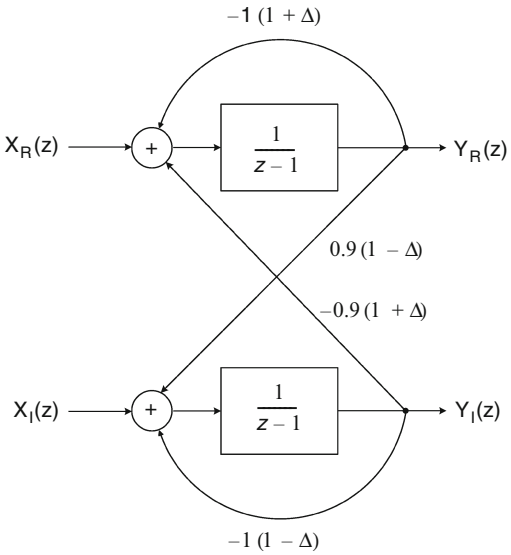


Fig. 4.2 (**a**) Signal flow diagram of a complex filter with mismatch, (**b**) Magnitude of the signal and image response for a single-pole complex filter with mismatch

4.2 Mismatches in a Complex ΔΣ Modulator

The coefficients in the system model of a ΔΣ modulator are mapped to capacitor ratios in the switched-capacitor (SC) circuit implementation. Due to process variations, the feed-in capacitors and the integrating capacitors may show variation from their desired values, and these variations manifest as errors in the realized coefficient values. In a ΔΣ modulator, these ratio-errors can cause the gains of the integrator stages to differ from their nominal values, and this difference may result in modification of the NTF zeros. In the worst case, this modification



$$H(z) = \frac{Y(z)}{X(z)} = \frac{1}{z-p}$$

$$p = 0.9\,e^{j(\pi/2)} = j0.9$$

$$\Delta = 0.1\,\%$$

Fig. 4.3 Realizing a complex pole at $p = p_r + jp_i$ using two-input two-output non-ideal linear signal flow graph

may cause a ΔΣ modulator to become unstable. Amplifiers implemented with opamps also vary in dc gain and settling characteristics from stage to stage or channel to channel.

In a complex ΔΣ modulator the circuit mismatches cause the real and the quadrature paths to differ, and this difference impacts the image rejection and the SNDR of the modulator. As discussed in Chap. 2, in addition to the signal transfer function (STF) and noise-transfer function (NTF), two additional transfer functions, refer to Fig. 4.4, are needed to describe the behavior of a complex ΔΣ modulator with mismatches in its coefficients [2]: (1) *Image noise transfer function* (INTF) that describes the transfer from the quantization noise in the image-band to in-band at the output of the modulator, and (2) *Image signal transfer function* (ISTF) that describes the transfer from the image-band signals at the input of the modulator to the in-band signals at the output of the modulator.

The STF determines the gain from the signal input to the output of the modulator

$$STF \rightarrow \qquad G'\left(e^{j\omega}\right) = \frac{Y\left(e^{j\omega}\right)}{X\left(e^{j\omega}\right)} \tag{4.1}$$

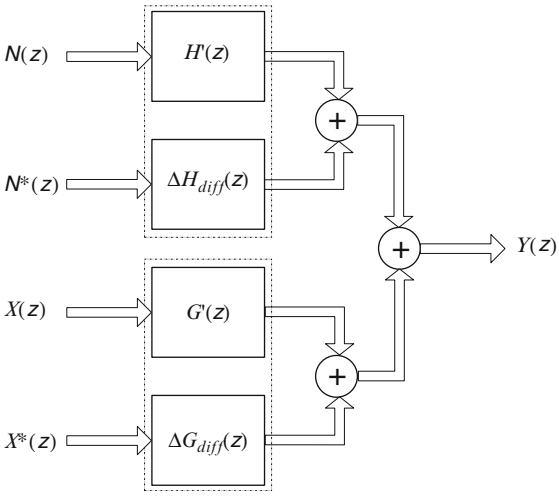


Fig. 4.4 Linear model of a complex ΔΣ modulator showing the four transfer functions that decide the output of the modulator in the presence of mismatches

The NTF determines the gain from the quantization-noise to the output of the modulator:

$$NTF \rightarrow \qquad H'\left(e^{j\omega}\right) = \frac{Y(e^{j\omega})}{N(e^{j\omega})} \tag{4.2}$$

ISTF determines the gain from the image-signal to the output of the non-ideal modulator:

$$ISTF \rightarrow \qquad \Delta G_{diff}\left(e^{j\omega}\right) = \frac{Y(e^{j\omega})}{X(e^{-j\omega})} \tag{4.3}$$

INTF determines the gain from the image-quantization noise to the output of the non-ideal modulator:

$$INTF \rightarrow \qquad \Delta H_{diff}\left(e^{j\omega}\right) = \frac{Y(e^{j\omega})}{N(e^{-j\omega})} \tag{4.4}$$

The impact of mismatches on the proposed complex ΔΣ modulator was simulated using the developed behavioral Simulink [3] model (refer to Appendix A).

Figure 4.5 shows the NTF and the INTF created by a mismatch of 0.5% in the modulator coefficients. As can be seen from the in-band zoom in Fig. 4.5b, the in-band noise has been shaped by deep in-band notches of the NTF. However, the quantization noise in the image-band is aliased by the INTF, whose gain in this particular case is comparable to that of the NTF. High-gain INTF implies that a very large amount of energy from out-of-band quantization noise is transferred into the in-band of the ΔΣ modulator.

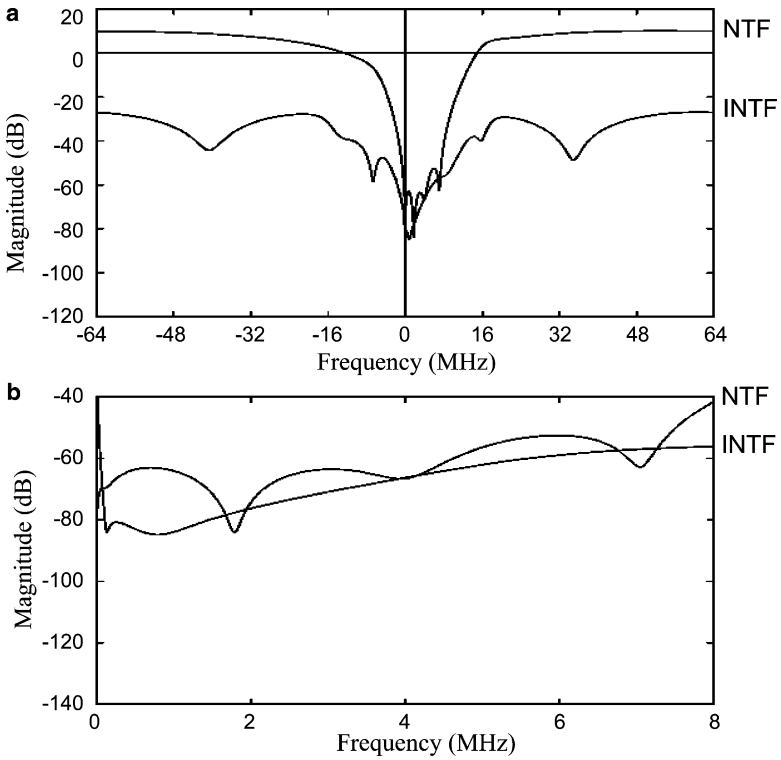


Fig. 4.5 (**a**) Transfer Functions –INTF and NTF, (**b**) Zoom-of the INTF and the NTF

Figure 4.6 shows the output spectrum for the same nonideal modulator for an input: $0.7\,e^{j2\pi\left(4\times10^6/128\times10^6\right)}$. Fig. 4.6c shows the in-band quantization noise (in black) and the aliased image-band quantization (in gray). The aliased image-band quantization is clearly larger than the in-band quantization noise, and this aliased noise may actually limit the SNR of the modulator. Figure 4.7 shows the STF and the ISTF created by a mismatch of 0.5% in the modulator coefficients. ISTF plays a critical role in transferring the image-band input signals into in-band signals at the output of the modulator. An image tone signal at the input of the modulator is shaped by ISTF. For the given modulator with 0.5% mismatch, in-band zoom in Fig. 4.7b indicates that the ISTF is about 50 dB below the ideal STF. This means that, assuming a linear-model, the image rejection for the modulator is 50 dB, in-band.

Figure 4.8 shows the response of the modulator for inputs in the signal-band and image-band. Fig. 4.8a shows the response of the modulator, without any mismatches, to a -20 dB two-tone signal at the image-frequency of -5 MHz and signal-band frequency of 6 MHz. In absence of any mismatches, the two tones can be seen at the output of the modulator, and there is no aliasing of the

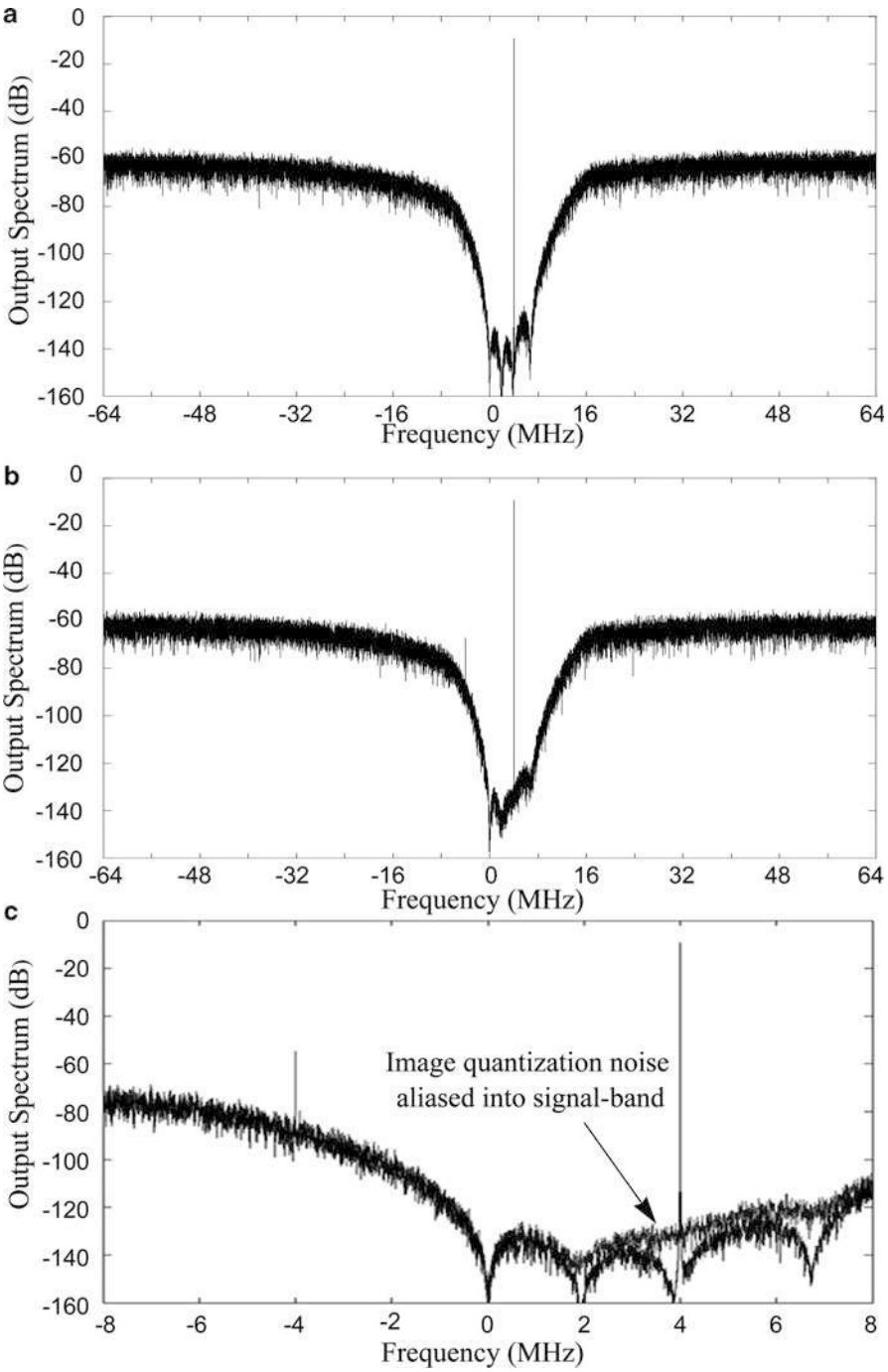


Fig. 4.6 Output spectrum: (**a**) Ideal spectrum (**b**) with 0.5% mismatch. (**c**) Zoom-in image quantization aliasing into signal-band

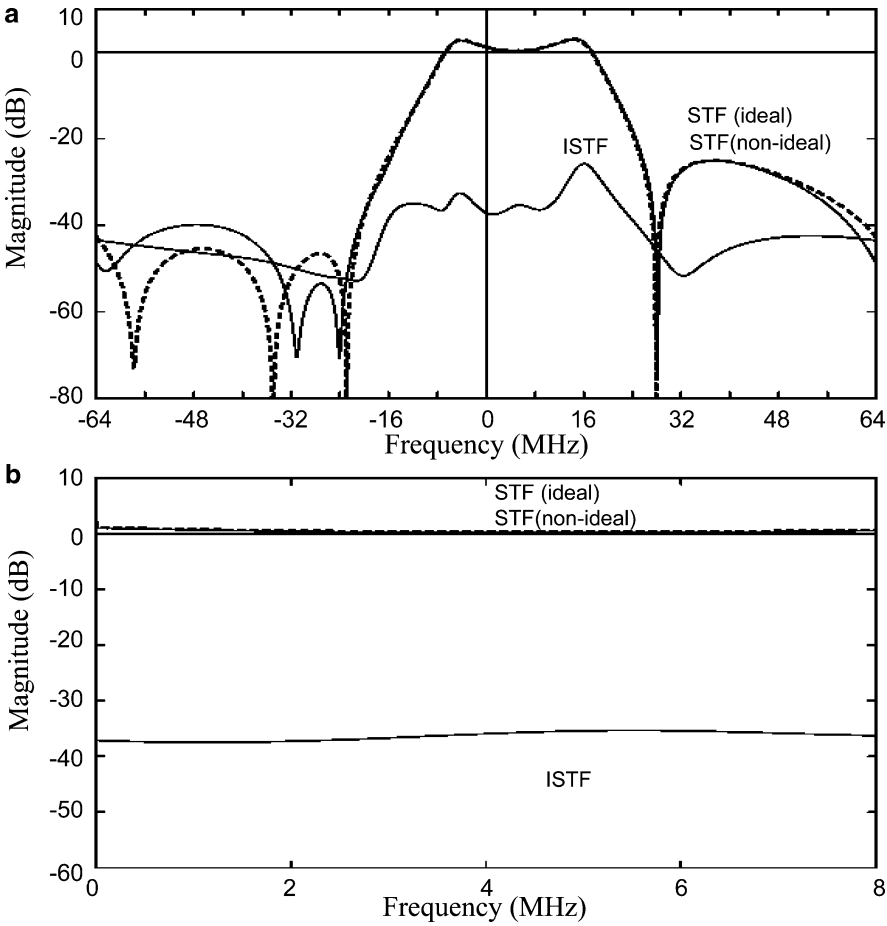


Fig. 4.7 (**a**) Transfer Functions – ISTF and STF, (**b**) Zoom-in of the ISTF and the STF

signal-band frequency to the image-band or vice versa. However, with $\pm 0.5\%$ mismatches added, the –20 dB image-frequency is shaped by the ISTF, and an aliased signal at –70 dB, 5 MHz, appears in the output spectrum, Figure 4.8b.

To determine the SNDR degradation of the modulator due to mismatches, Monte Carlo simulations were run with amplifier nonidealities, and a differential error of $\pm 0.5\%$ added to all gain and complex pole parameters. Figure 4.9a,b show in-band transfer functions for 200 Monte Carlo simulations. Figure 4.9a shows NTF and INTF curves for the modulator. Compared to the NTF curves, the INTF shows wider variation and can be responsible for transferring out-of-band noise to the in-band region. Figure 4.9b shows the STF and ISTF curves for the modulator. The in-band variation of the STF is less than 1 dB.

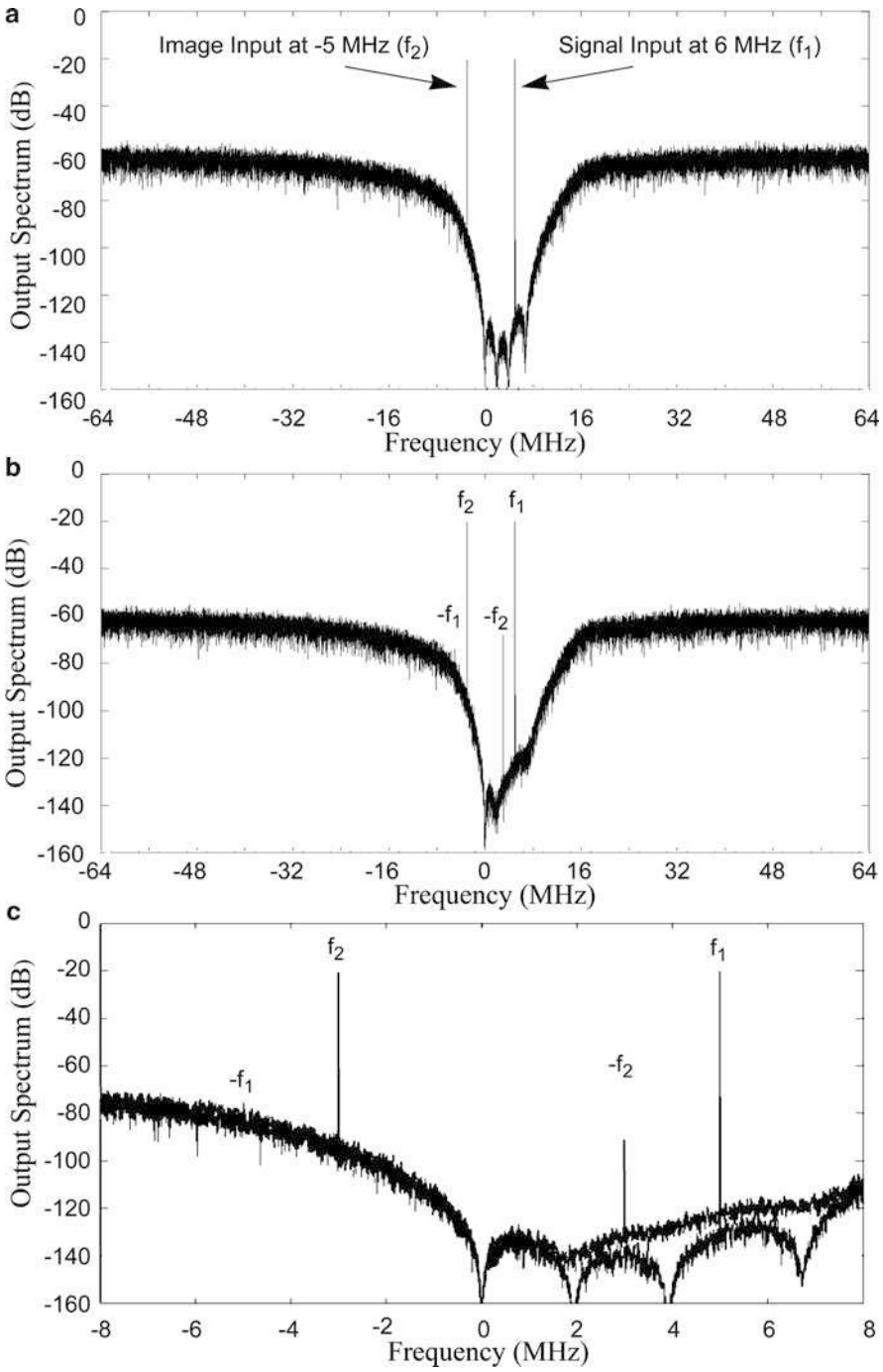


Fig. 4.8 Output spectrum with a signal-band tone and an image-band tone: (**a**) Ideal spectrum, (**b**) with 0.5% mismatch, (**c**) Zoom-in of image-tone aliasing into the signal-band

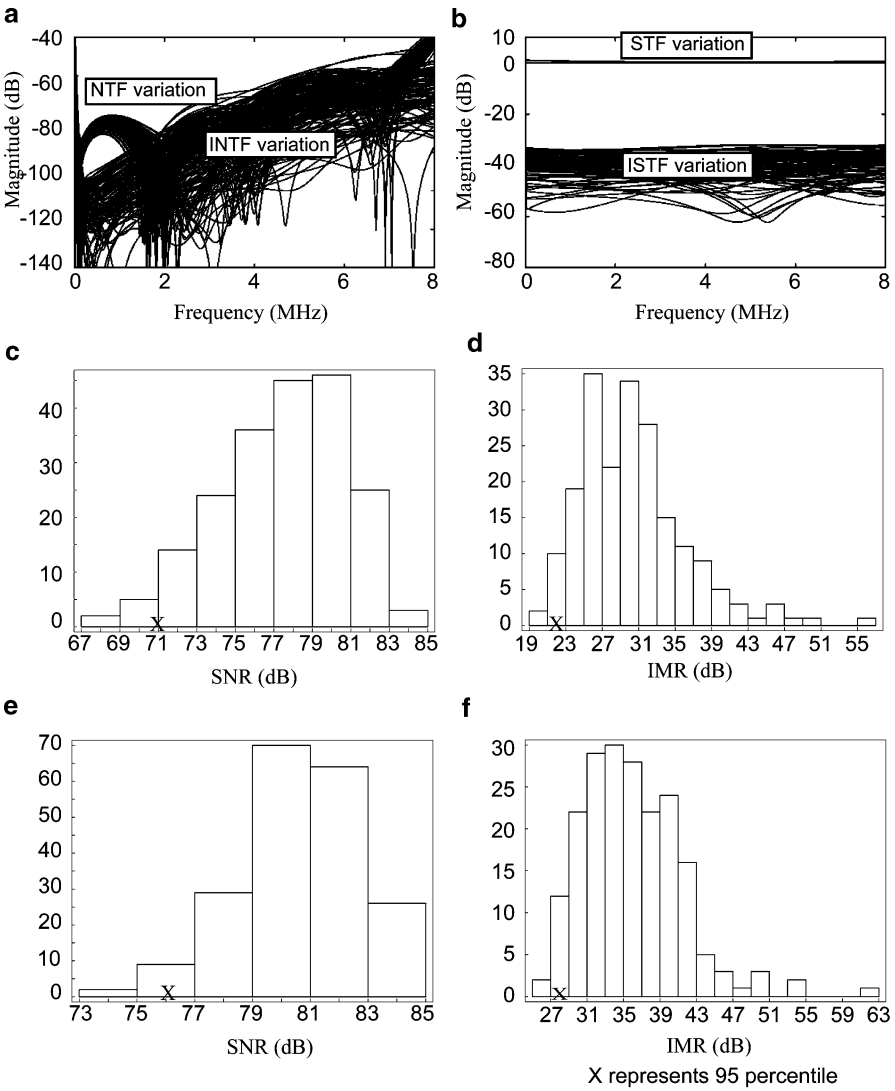


Fig. 4.9 Transfer functions for the original modulator: (**a**) NTF and INTF variation for $\pm 0.5\%$ random mismatch, (**b**) STF and ISTF variation for $\pm 0.5\%$ random mismatch. Histograms for (**c**) SNR and (**d**) IMR for the modulator with $\pm 0.5\%$ random mismatch. Histograms for (**e**) SNR and (**f**) IMR for the modulator with $\pm 0.25\%$ random mismatch

The ISTF starts at approximately 50 dB below the STF; however, closer to the signal band-edge the distance progressively decreases to 40 dB. This implies greater than 50 dB image-rejection, which however deteriorates to 40 dB for signals closer to the band-edge. This conclusion about image-rejection is based on

a linear model for the modulator; however, actual image rejection will need to be determined through full simulations. Monte Carlo simulations of the modulator with ± 0.5% coefficient mismatch and finite dc-gain nonidealities of the amplifier modeled were performed to generate the SNR and IMR histograms shown in Fig. 4.9c, d. An another set of simulations with the same amplifier nonidealities, however the peak mismatch decreased to ± 0.25% were performed to generate the histograms shown in Fig. 4.9e, f. For ±0.25% random mismatches, 95% of the modulators achieve SNR greater than 71 dB and IMR greater than 21 dB. For ±0.5% coefficient- mismatches, the minimum SNR drops to 67 dB, which is a loss of 14 dB from the ideal case.

4.2.1 An Improved Complex ΔΣ Modulator

A technique to reduce SNR degradation due to image quantization noise aliasing into the signal-band is to move one of the NTF zeros to the image frequencies [2]. The advantage of this method is that the image zero suppresses the image band quantization noise before it aliases into the signal-band. However, sacrificing one of the NTF zeros means reduction in the suppression of the in-band quantization noise; effectively, thus reducing the order of the modulator.

In the modified ΔΣ modulator, one of the NTF zeros has been placed in the center of the image-band (–4 MHz). For a fourth-order modulator, there is apparently a flexibility in choosing the stage in which to realize the image zero, but, it turns out that technique offers significant improvement over the original modulator only when the image-zero is realized in the third or the fourth stage. The significance of stage-ordering for complex filters can be understood from the fact that, under mismatches, complex filters are not commutable; for example, a complex filter, *AB*, made of stage *A* followed by stage *B*, is not same as a complex filter, *BA*, made of stage *B* followed by stage *A*. The order in which the in-band zeros are realized has a negligible impact on the INTF variation.

Figure 4.10a shows the pole-zero plot of the modified ΔΣ modulator. An NTF zero has been moved to the image-frequency of –4 MHz. Figure 4.10b, c show the NTF magnitude response and the zoom-in view of the image-band and the signal-band. Figure 4.11a shows the 64k-bin output spectrum of the modified complex ΔΣ modulator. The output PSD plot shows three notches in the signal-band and a single notch in the image-band. Figure 4.11c shows the zoom-in of the signal-band for a random ±0.5% coefficient mismatch. Compared with Fig. 4.8c, Fig. 4.11c shows that negligible image-band quantization noise has aliased into the signal band.

Compared to the ideal ΔΣ modulator with all the NTF zeros distributed over the signal- band (0–8 MHz), the modified ΔΣ modulator shows lower SNR. This SNR degradation is due to the NTF which is effectively 3rd order now. However,

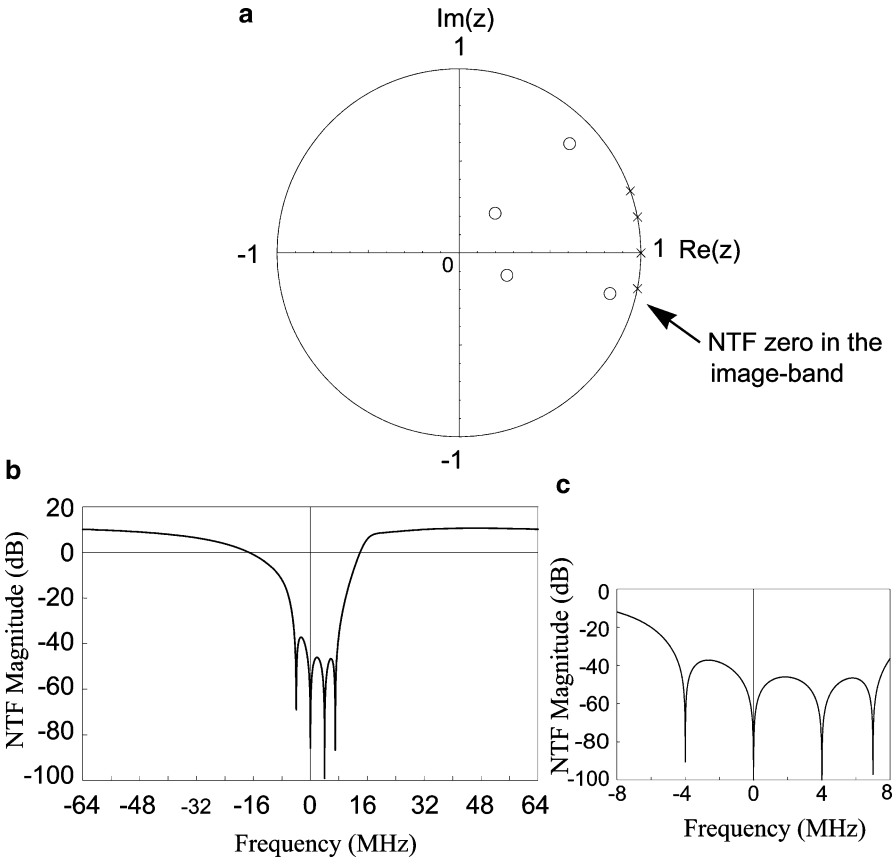


Fig. 4.10 The modified ΔΣ Modulator: (**a**) NTF pole-zero plot, (**b**) NTF magnitude response, (**c**) Zoom-in of the signal-band and image-band

the modified ΔΣ modulator shows an increased robustness and relatively small SNR degradation due to coefficient mismatch. Compared to the worst SNR degradation of 11.74 dB and 10.47 dB for ±0.5% and ±0.25% coefficient mismatches respectively, for the original modulator, the modified modulator shows an SNR degradation of 2.8 dB and 1.9 dB for the same coefficient mismatches. (Refer to Fig. 4.12.)

Introduction of a zero in the image-band has relatively little impact on the shape of the ISTF, and the expectation is that the image-rejection of the modulator should remain unaffected by this method. Mismatch simulations (Fig. 4.12b) reveals that the ISTF variation of the modified modulator is close to the original modulator.

Table 4.1 summarizes the comparison between the original modulator and the improved modulator.

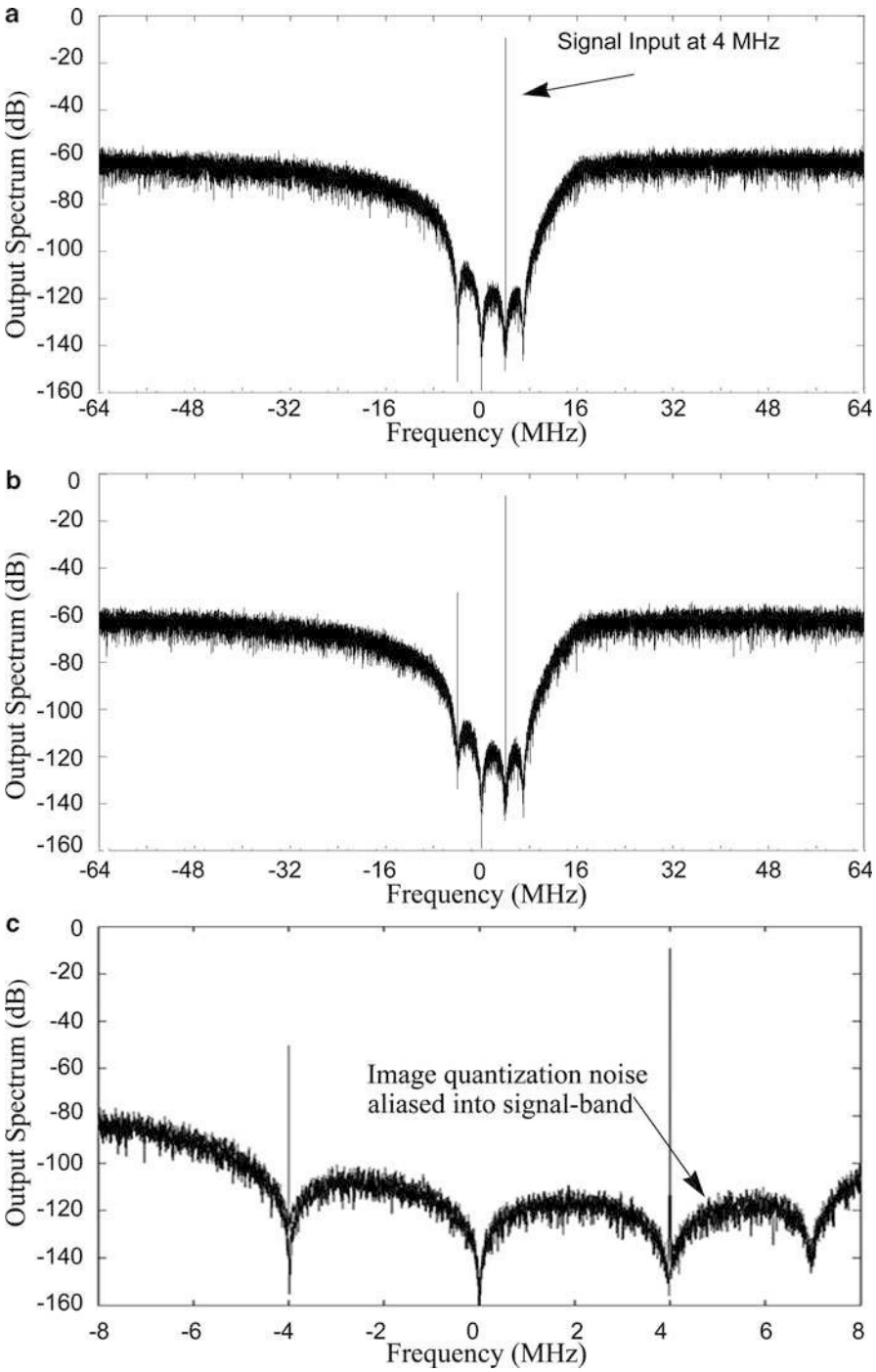


Fig. 4.11 Output spectrum of the modified modulator: (**a**) Ideal spectrum, (**b**) with 0.5% mismatch, (**c**) Zoom-in of image quantization aliasing into signal-band

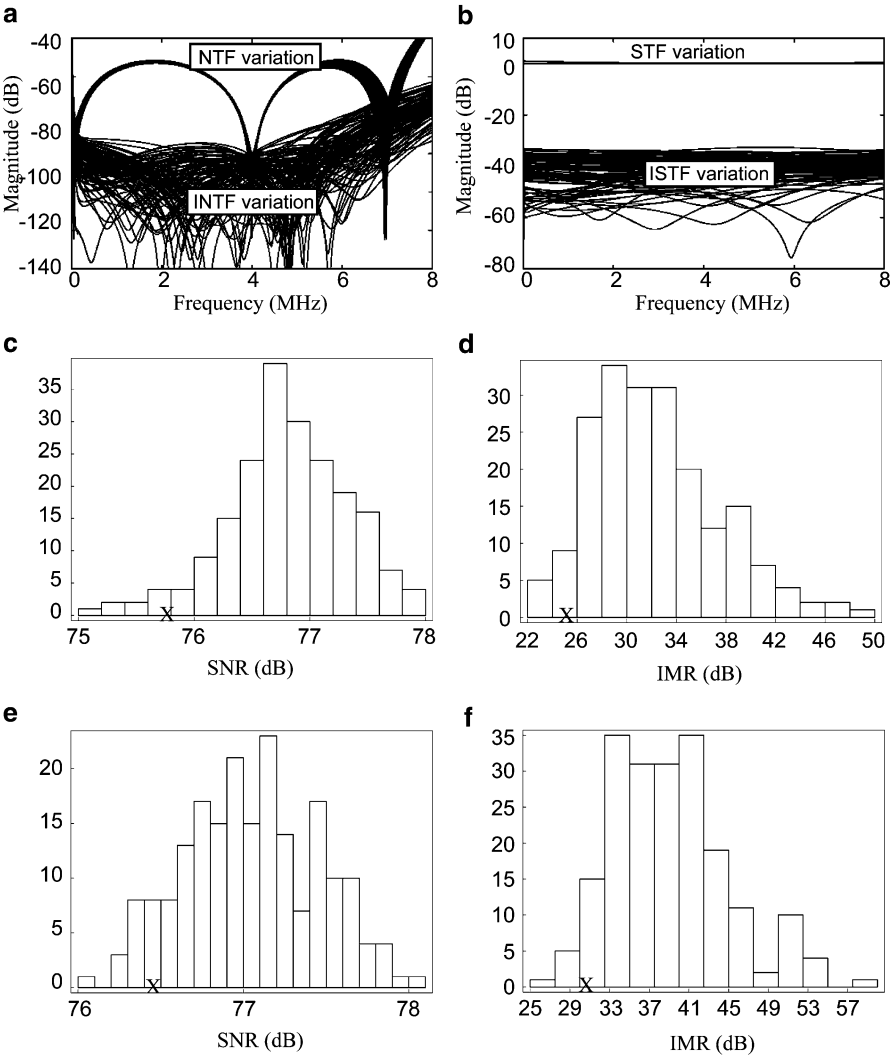


Fig. 4.12 Transfer functions for the modified modulator: (**a**) NTF and INTF variation for $\pm 0.5\%$ random mismatch, (**b**) STF and ISTF variation for $\pm 0.5\%$ random mismatch. Histograms for (**c**) SNR and (**d**) IMR for the modulator with $\pm 0.5\%$ random mismatch. Histograms for (**e**) SNR and (**f**) IMR for the modulator with $\pm 0.25\%$ random mismatch

Table 4.1 Simulated modulator performance with $\pm 0.5\%$ mismatch

	Original modulator	Modified modulator
SNR (ideal)	81 dB	77 dB
SNR (95th-percentile)	71 dB	76 dB
IMR (95th-percentile)	23 dB	25 dB

4.3 The Switched-Capacitor Architecture

4.3.1 Complex Integrators

A complex integrator is created by two cross-coupled real integrators, as shown in Fig. 4.13. The nondelaying complex integrator of the proposed ΔΣ modulator has been realized by two non-delaying SC integrators. As the SC implementation is fully-differential, the negative valued cross-coupling coefficient is realized by reversing the connection to the differential amplifier outputs. The ratio of the feedback capacitor, C_d, to the integration capacitor, C_i, sets the real part of the complex zero, and the ratio of C_d to C_i sets the imaginary part of the complex zero. Figure 4.14 shows realization of a delaying complex integrator by two delaying SC integrators.

4.3.2 Dynamic Range Scaling

For an SC modulator, the voltage swing at an integrator output is limited by the output saturation voltages of the opamps. The ΔΣ modulator Simulink model was simulated for different input frequencies and amplitudes in order to obtain the peak values at each integrator output. To ensure that each opamp output never exceeded the reference levels, dynamic range scaling was performed by multiplying the coefficients at an integrator input by a factor and dividing the coefficients at the output of the integrator by the same factor [1]. In the Simulink model, for a –6 dB input signal, the peak values at the integrator outputs were limited to 70% of the reference levels.

The reference levels to the multibit quantizer and the multilevel DAC are set at 1.4 V and 0.4 V, and centered around a common-mode of 0.9 V. With Dynamic range scaling, each opamp is limited to a maximum differential swing of 1.4 $V_{p\text{-}p}$.

4.3.3 Multibit Quantization

During the noise assignment of the modulator (see Sec. 4.4.1.2), 25% of the total permissible noise was assigned to in-band quantization noise. At an OSR of 16, a 4-bit quantizer is required to suppress the in-band quantization-noise to the required level that is, below the noises from the analog circuit and other sources. Behavioral simulations with a 4-bit quantizer predict a peak signal-to-quantization ratio ($SQNR_{peak}$) of 81 dB for an overload-ratio (A_{OL}) [4] of 0.75.

In the proposed ΔΣ modulator implementation, the 4-bit quantizer will be implemented as a 15-level flash ADC. Behavioral Monte Carlo simulations show that the modulator is robust to quantizer offsets, and even an offset of value 20 mV has a negligible impact on the SNR of the modulator.

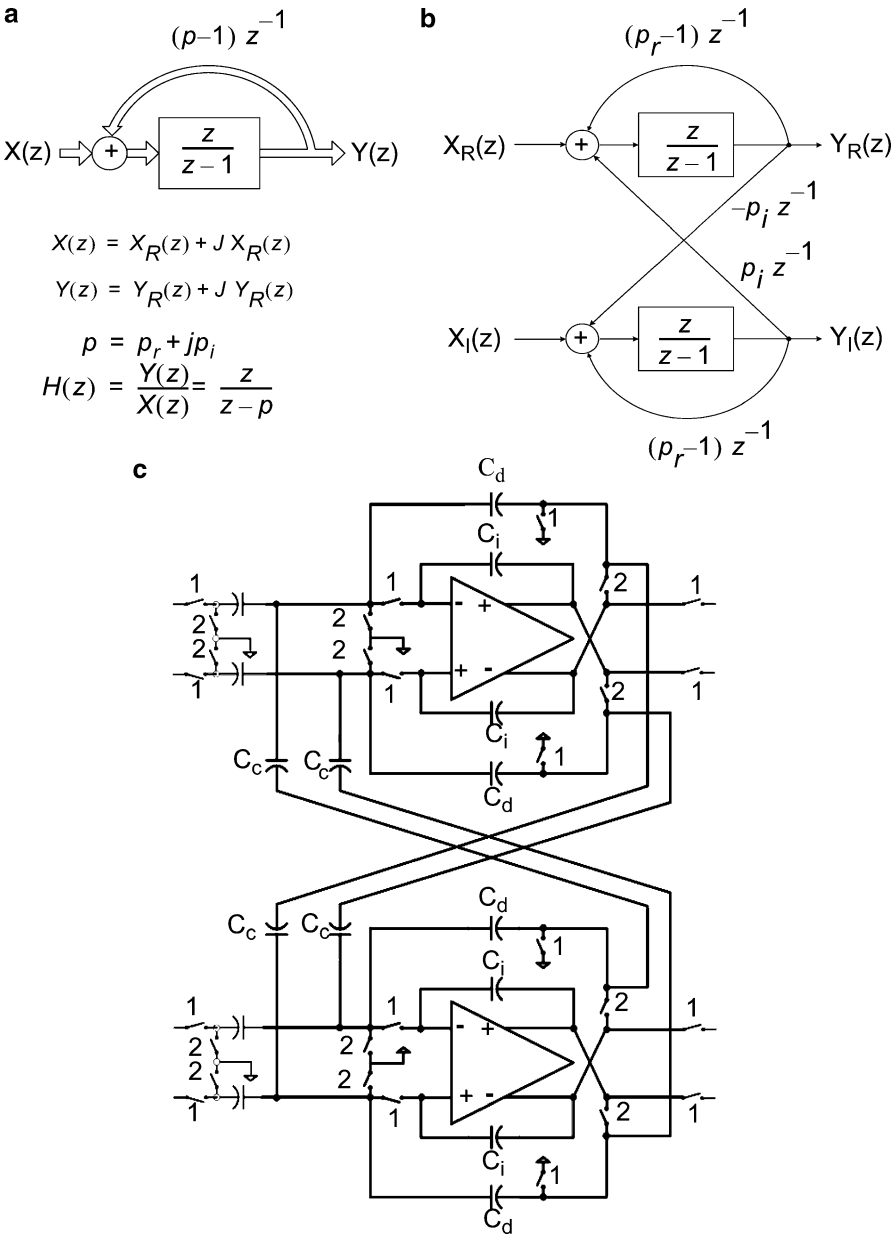


Fig. 4.13 Realization of a complex pole at $p = p_r + jp_i$ using (**a**) a complex signal flow graph and (**b**) a two-input two-output real linear signal flow graph. (**c**) a fully-differential SC realization of the nondelaying complex integrator

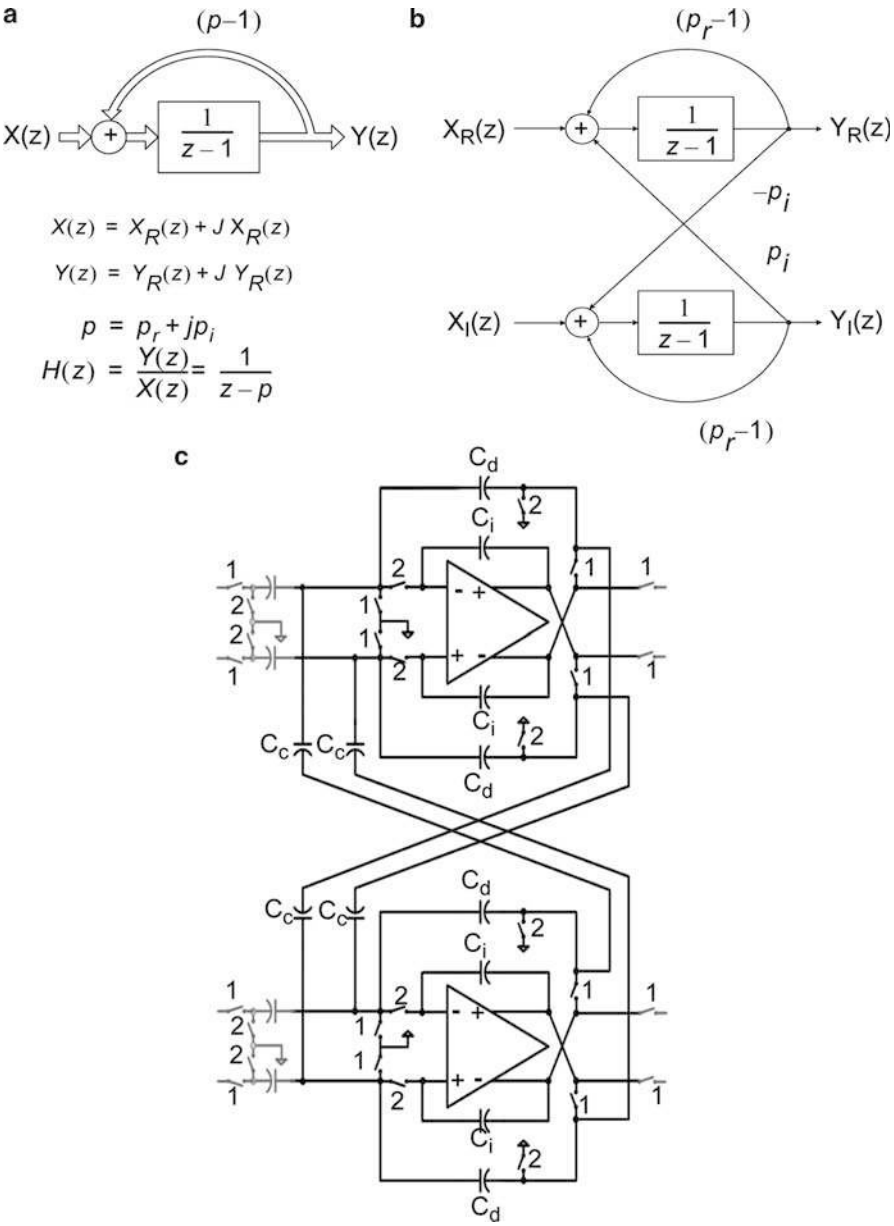


Fig. 4.14 Realization of a complex pole at $p = p_r + jp_i$ using (**a**) a complex signal flow graph and (**b**) A two-input two-output real linear signal flow graph. (**c**) A fully-differential SC realization of the delaying complex integrator

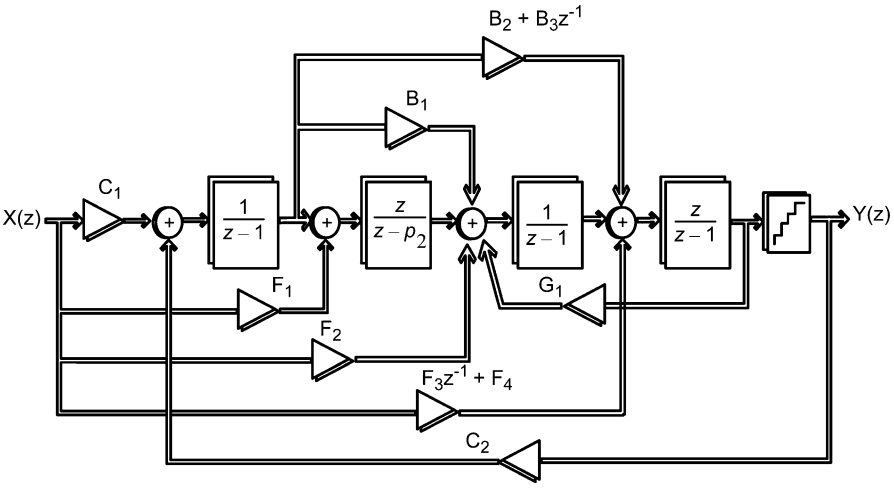


Fig. 4.15 Architecture of the modified ΔΣ modulator

4.3.4 Multilevel DAC

The proposed complex ΔΣ modulator uses one multilevel DAC in the feedback loop. The complex feedback coefficient, C_2, in Fig. 4.15 is realized by a real and an imaginary array of 15 capacitors each (refer to Figure 4.16). The thermometer output code of the quantizer is connected to the switched-capacitor feedback DAC. To account for the effect of capacitor mismatches in the DAC unit capacitors, the behavioral model of the modulator was simulated with mismatch error in the DAC elements. Section 4.4.1 reports the worst-case SNDR performance due multilevel DAC nonlinearity found over 100 simulations of the modulator.

4.3.5 Realizing the Feedins

In Figure 4.13, the coefficient F_3 realizes an input feed-in term delayed by one clock cycle before it is added to other inputs of the last integrator. To implement F_3, the combined feed-in terms F_3 and F_4 were implemented as the summation of a nondelayed term and a differentiator term:

$$F_3 z^{-1} + F_4 = F_3 + F_4 - F_3\left(1 - z^{-1}\right)$$

Similarly, to reduce the coefficient spread for the coefficients B_2 and B_3, the feed-forward $B_2 + \mathrm{B}_3\, z^{-1}$ was implemented as Table 4.2:

$$B_2 + B_3 z^{-1} = B_2 + B_3 - B_3\left(1 - z^{-1}\right)$$

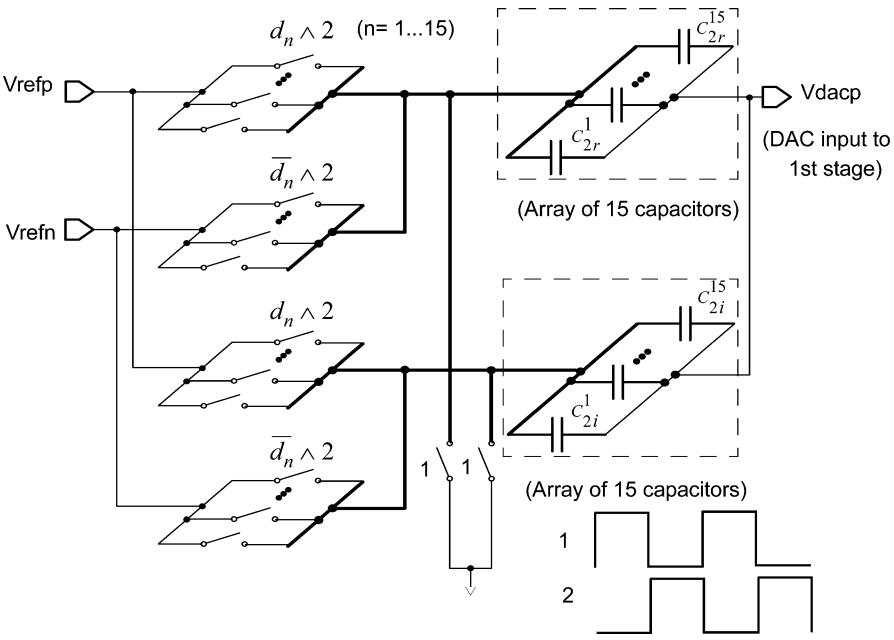


Fig. 4.16 Multi level DAC

Table 4.2 Implementation of the feed-ins and the feed-forward coefficients

Initial coefficient values	Modified coefficient Values
$F_3 = -0.32 - 0.67I$	$F_3 + F_4 = -0.3 - 0.67I$
$F_4 = 0.02$	$-F_3 = 0.32 + 0.67I$
$B_2 = 2.0 + 3.93I$	$B_2 + B_3 = 1.15 + 2.04I$
$B_3 = -0.93 - 1.88I$	$-B_3 = 0.93 + 1.88I$

4.3.6 The Complete Fully-Differential SC Architecture

Figure 4.17 shows a single-ended representation of the SC implementation of the complex ΔΣ modulator. The actual circuit implemented is fully-differential. The NTF zero at dc is realized by the first stage. The second stage with complex feedins realizes the complex NTF zero, and the zeros at the image frequency and the centre of the signal passband are realized by the real resonator, that is, stage three and stage four. Each channel output goes to a 4-bit quantizer. The two 4-bit quantizers generate a 15-bit thermometer code, which is connected to a switched-capacitor feedback DAC. The feedback DAC implements a complex coefficient that uses a real and an imaginary array of 15 capacitors each, with the smallest unit capacitor sizes equal to 24 ff (real) and 25.7 ff (imaginary) respectively.

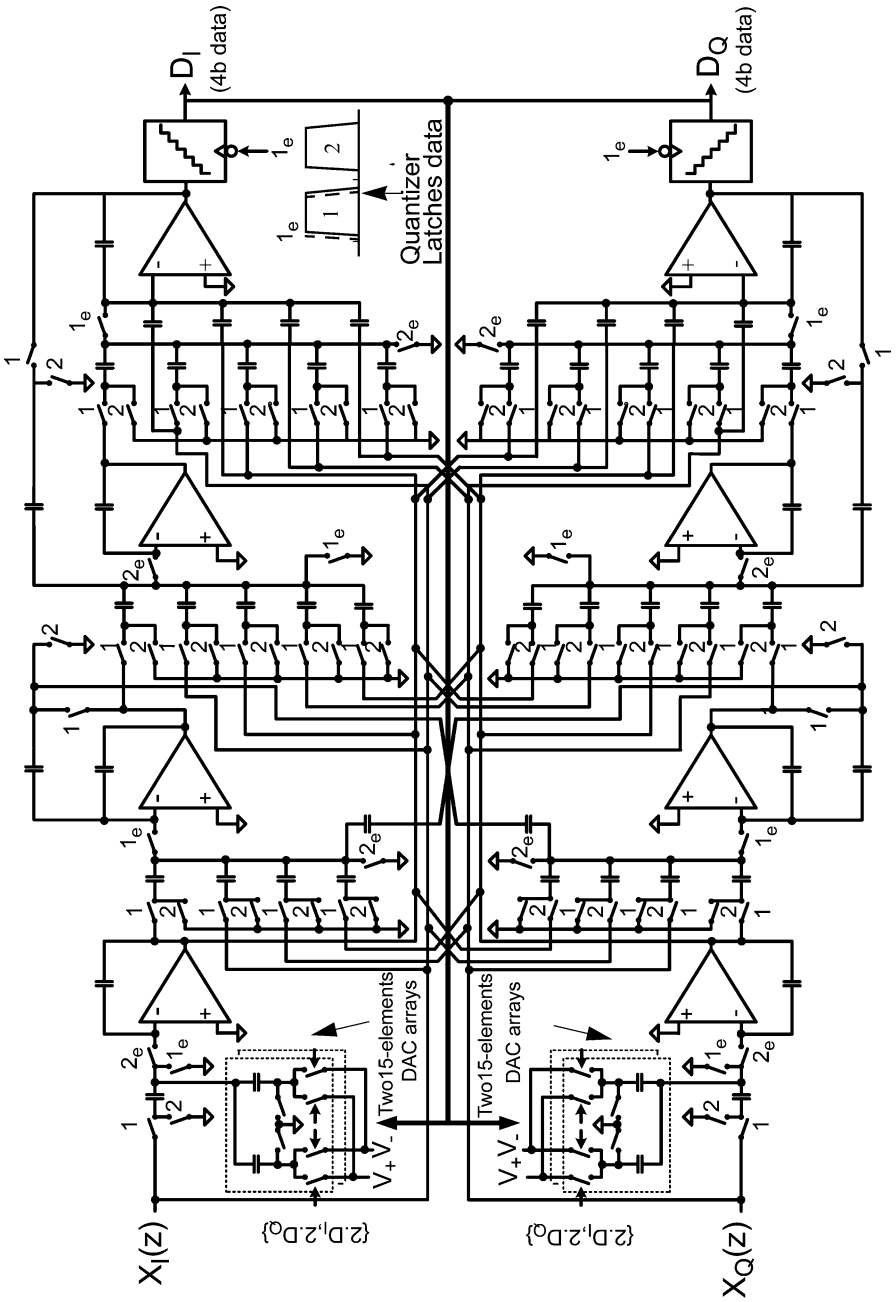


Fig. 4.17 Single-ended representation of the SC implementation of the complex ΔΣ modulator

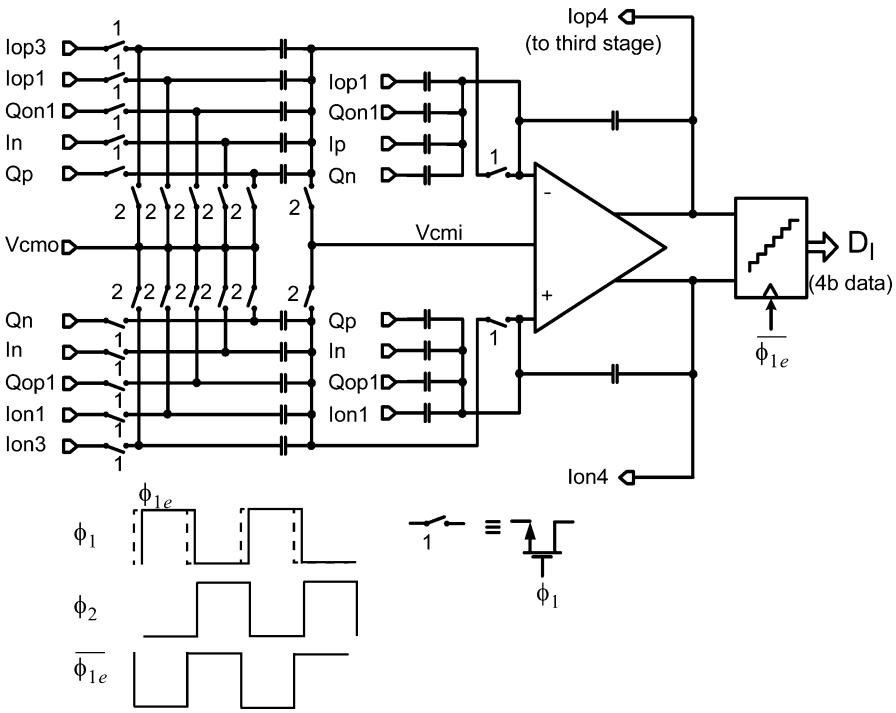


Fig. 4.18 Clocking scheme- real-channel fourth-stage and the quantizer

4.3.7 The Clocking Scheme

The ΔΣ ADC uses two non-overlapping clock phases, ϕ_1 and ϕ_2, and their "early" versions, ϕ_{1e} and ϕ_{2e}, to minimize charge-injection [5]. A nonoverlapping clock generator provides the necessary clock phases.

The first stage of the modulator samples input during clock phase ϕ_1, and the feedback DAC applies the references during clock phase ϕ_2. Figure 4.18 shows the fully-differential implementation and clocking for the fourth-stage amplifier and the 4-bit quantizer.

4.4 System-level Behavioral Simulations

4.4.1 Capacitor Sizing

4.4.1.1 Capacitor Mismatch

In an SC ΔΣ modulator, the integrator gains are implemented by capacitor ratios. Process variations cause the realized capacitors to deviate from their nominal values. For example, for a coefficient of value G realized as a ratio

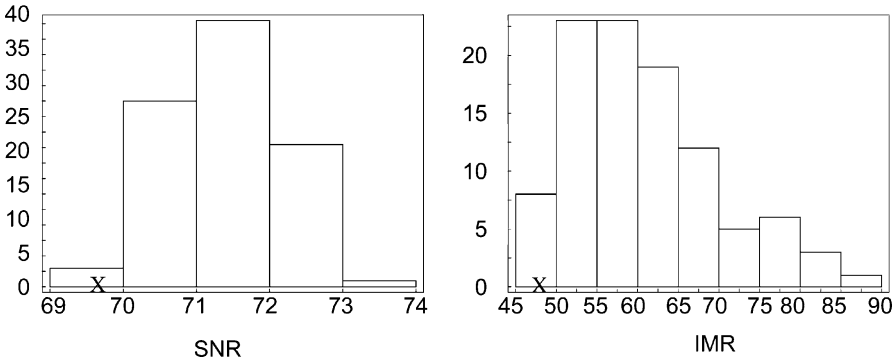


Fig. 4.19 Histograms for (**a**) SNR and (**b**) IMR for the proposed ΔΣ modulator with ± 0.5% random coefficient mismatch in the DAC elements

of two capacitors, Cg and C_i, the actual implemented coefficient value, G^*, is given by:

$$G^* = \frac{C_g\left(1 + \frac{A_c}{\sqrt{m\,(WL)_g}}\right)}{C_i\left(1 + \frac{A_c}{\sqrt{n(WL)_i}}\right)} \tag{4.5}$$

where A_c is a process-dependent parameter.[1] The deviations of the coefficients from their nominal values are manifest as a modification of the NTF and STF of the modulator. A technique intended to realize capacitor ratios with higher accuracy is implementation by capacitors realized as an array of unit capacitors. Behavioral simulations of the modulator were used to identify the sensitive coefficients, and the capacitors realizing these coefficients were sized larger in order to minimize their deviations.

The multilevel DAC has been implemented as an array of unit capacitors. Errors in the values of these unit capacitors can limit the linearity and resolution of the ΔΣ modulator. To account for the effect of capacitor mismatches in the DAC unit capacitors, over 100 behavioral simulations, with random mismatches of ± 0.5% peak-value in the DAC unit elements, were performed to examine the worst case SNDR and IMR.

For ± 0.5% mismatch values, the minimum SNDR falls to 69.7 dB with 95-percentile at 70 dB. The minimum IMR drops to 46.2 dB, with 95-percentile of the IMR at 48.6 dB (Fig. 4.19).

However, when realistic mismatch values based on the process mismatch factor and (4.5), and also the capacitor values derived in Sec. 1.4.0.1 are used,

[1] This assumes that the area effects dominate and the edge effects can be ignored.

($C_{C2R} = 23.2 \times 15 = 348fF, C_{C2I} = 51.4 \times 15 = 771.5fF, C_i = 1.9pF$), the actual mismatch for the DAC coefficients, $C_{2R}\,C_{2I}$, comes out to less than $\pm 0.1\%$. For $\pm 0.1\%$ mismatch in the feedback coefficient, the minimum SNR comes out at 77.5 dB, with 95-percentile at 78 dB. The minimum IMR for $\pm 0.1\%$ mismatch is at 58.2 dB, with 95-percentile at 62.65 dB.

4.4.1.2 Noise Analysis

Thermal noise estimation for a complex ΔΣ modulator is similar to noise estimation for a low-pass ΔΣ modulator. The noise estimation in a ΔΣ modulator starts with the identification of the thermal noise sources, for example, SC switches, opamps in the circuit [6]. For example, Fig. 4.20a shows a complex integrator with two uncorrelated noise sources, V_{nI1} and V_{nI2}, but both having the same power added to represent the switch noise sources in the cross-coupling SC branches. Similarly, V_{nI1} and V_{nI2} in the Fig. 4.20 represent switch noise sources in the feedback branches of the integrator. It can be shown that the noise sources V_{nI2} and V_{nI2} can be combined into a single noise source V_{nI} in a simpler signal-flow graph representation of the complex integrator (Fig. 4.20b), where V_{nI} is given by:

$$V_{nI} = (p_r - 1)\sqrt{\frac{kT}{C_c}\frac{2x+1}{x+1}} \tag{4.6}$$

The multiplying factor $\frac{2x+1}{x+1}(x = 2g_m r_{on})$ in the equation represents the reduction due to the finite bandwidth of the opamp. Similarly, in Fig. 4.20b, the noise sources V_{nR1} and V_{nR2} have been combined into a noise source V_{nR}, where V_{nR} is given by:

$$V_{nR} = (p_i)\sqrt{\frac{kT}{C_d}\frac{2x+1}{x+1}} \tag{4.7}$$

Figure 4.20b shows the equivalent noise representation for a complex integrator; the SC branch switch noises have been combined with the opamp noises V_{Opamp1} and V_{Opamp2}, which represent thermal flicker and other noises generated in the opamp devices.

Figure 4.21 shows the block diagram of the complex ΔΣ modulator, with thermal noise sources added at the inputs of the feed-ins to the integrators. For an integrator stage, the opamp noise after proper scaling can be combined with one of the feed-in noise sources. Figure 4.22 shows the frequency responses of the power transfer functions for each noise source to the output of the modulator. For a complex coefficient, there are two transfer functions corresponding to the real and the imaginary parts of the coefficient. Integration of each power transfer function from dc to the signal-band edge represents the gain of the noise source

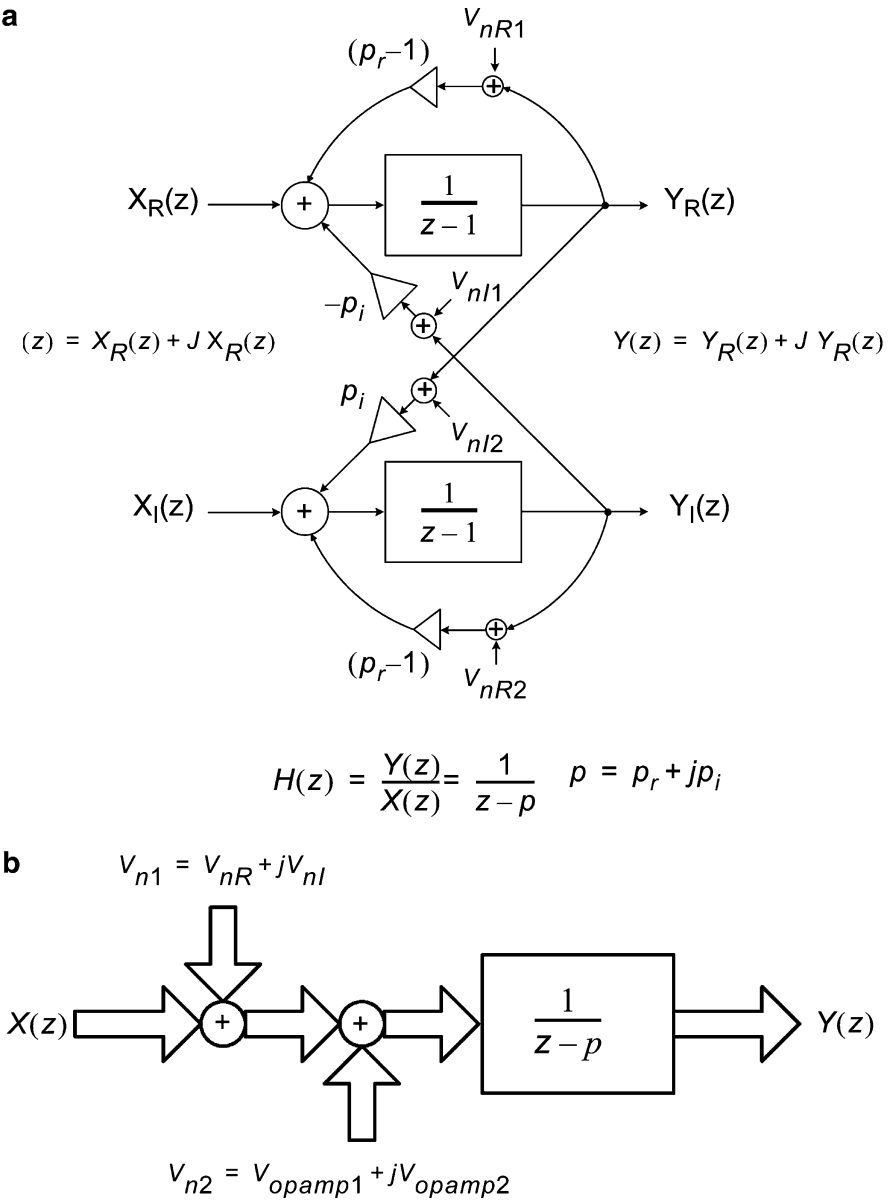


Fig. 4.20 Representation of noise sources in a complex integrator: (**a**) SC switch noise sources added to the complex signal flow graph, and (**b**) an equivalent noise representation in a signal-flow graph, including noise due to opamp devices

to the output of the modulator. Since the complex ΔΣ modulator has been designed with a unity STF in the signal-band, the input-referred noise power is equal to the output-referred noise power.

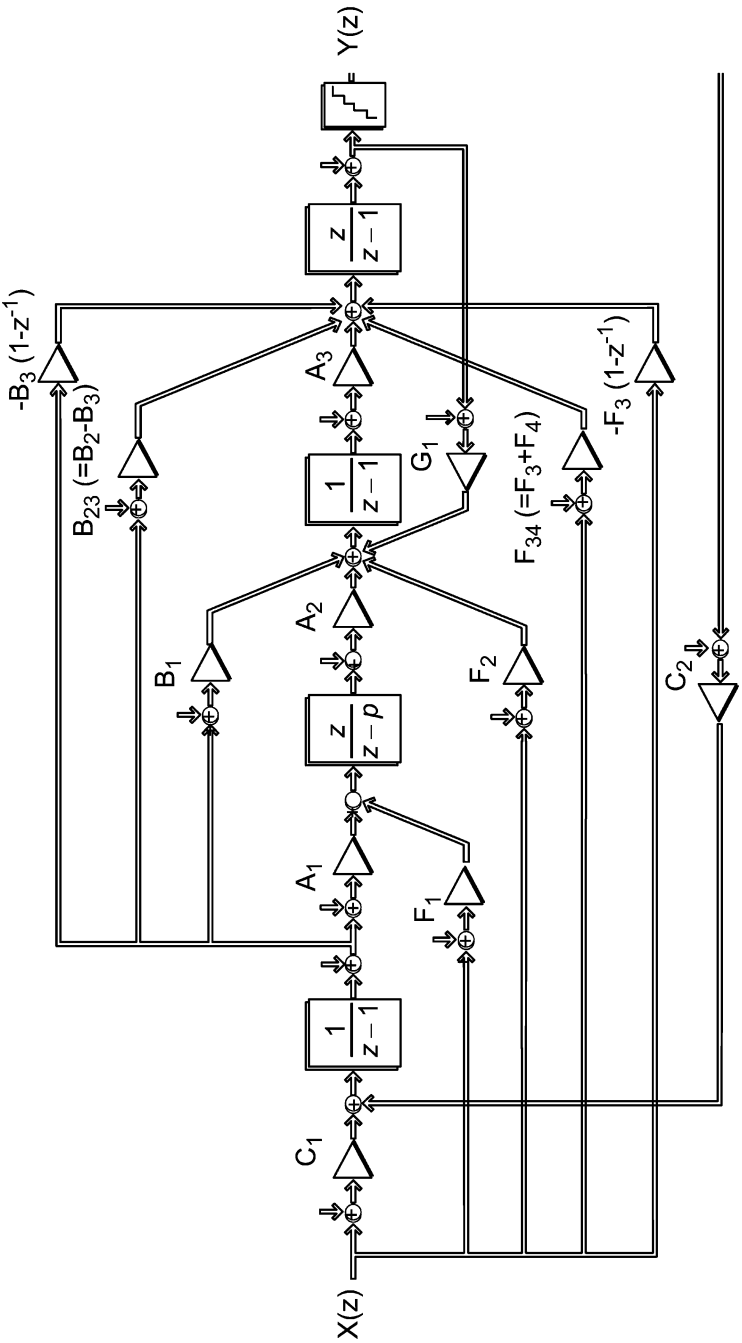


Fig. 4.21 Noise sources added to the complex $\Delta\Sigma$ modulator

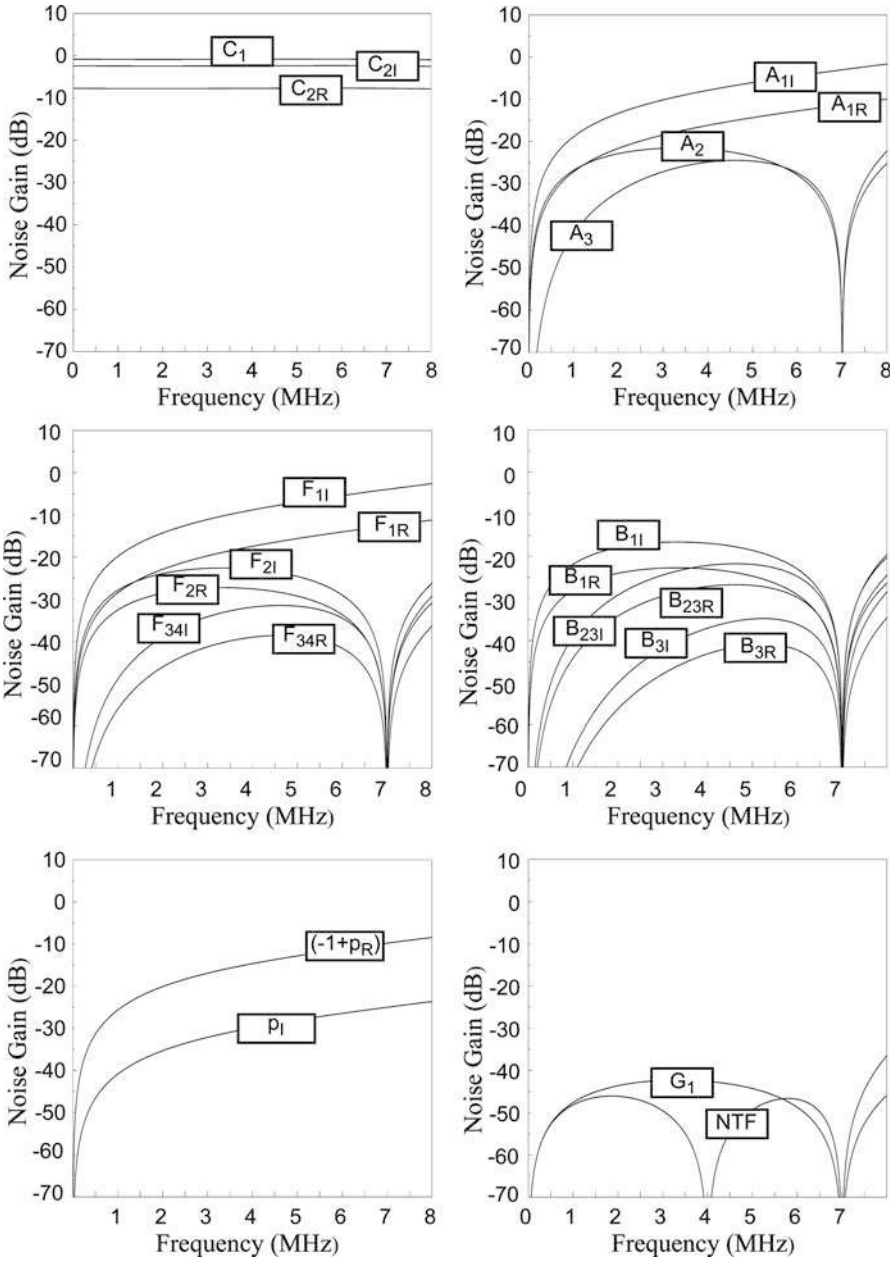


Fig. 4.22 Frequency responses of the noise transfer functions

The noise power spectral densities multiplied by the power transfer functions are given by:

$$
\begin{aligned}
\overline{v_n^2} = {} & \frac{\overline{v_{nC_1}^2}}{f_s/2} \int^{f_s/OSR} |NTF_{C_1}|^2\, df + && \leftarrow C_1 \\
& + \frac{\overline{v_{nC_{2R}}^2}}{f_s/2} \int^{f_s/OSR} |NTF_{C_{2R}}|^2\, df + \frac{\overline{v_{nC_1}^2}}{f_s/2} \int^{f_s/OSR} |NTF_{C_{2I}}|^2\, df && \leftarrow C_2 \\
& + \frac{\overline{v_{nA_{1R}}^2}}{f_s/2} \int^{f_s/OSR} |NTF_{A_{1R}}|^2\, df + \frac{\overline{v_{nA_{1I}}^2}}{f_s/2} \int^{f_s/OSR} |NTF_{A_{1I}}|^2\, df && \leftarrow A_1 \\
& + \frac{\overline{v_{nA_2}^2}}{f_s/2} \int^{f_s/OSR} |NTF_{A_2}|^2\, df && \leftarrow A_2 \\
& + \frac{\overline{v_{nA_3}^2}}{f_s/2} \int^{f_s/OSR} |NTF_{A_3}|^2\, df && \leftarrow A_3 \\
& + \frac{\overline{v_{nF_{1R}}^2}}{f_s/2} \int^{f_s/OSR} |NTF_{F_{1R}}|^2\, df + \frac{\overline{v_{nA_{1R}}^2}}{f_s/2} \int^{f_s/OSR} |NTF_{F_{1I}}|^2\, df && \leftarrow F_1 \\
& + \frac{\overline{v_{nF_{2R}}^2}}{f_s/2} \int^{f_s/OSR} |NTF_{F_{2R}}|^2\, df + \frac{\overline{v_{nF_{2I}}^2}}{f_s/2} \int^{f_s/OSR} |NTF_{F_{2I}}|^2\, df && \leftarrow F_2 \\
& + \frac{\overline{v_{nF_{34R}}^2}}{f_s/2} \int^{f_s/OSR} |NTF_{F_{34R}}|^2\, df + \frac{\overline{v_{nF_{34I}}^2}}{f_s/2} \int^{f_s/OSR} |NTF_{F_{34I}}|^2\, df && \leftarrow F_{34} \\
& + \frac{\overline{v_{nB_{1R}}^2}}{f_s/2} \int^{f_s/OSR} |NTF_{B_{1R}}|^2\, df + \frac{\overline{v_{nB_{1I}}^2}}{f_s/2} \int^{f_s/OSR} |NTF_{B_{1I}}|^2\, df && \leftarrow B_1 \\
& + \frac{\overline{v_{nB_{23R}}^2}}{f_s/2} \int^{f_s/OSR} |NTF_{B_{34R}}|^2\, df + \frac{\overline{v_{nB_{23R}}^2}}{f_s/2} \int^{f_s/OSR} |NTF_{B_{23R}}|^2\, df && \leftarrow B_{23} \\
& + \frac{\overline{v_{nB_{3R}}^2}}{f_s/2} \int^{f_s/OSR} |NTF_{B_{3R}}|^2\, df + \frac{\overline{v_{nB_{3I}}^2}}{f_s/2} \int^{f_s/OSR} |NTF_{B_{3I}}|^2\, df && \leftarrow B_3 \\
& + \frac{\overline{v_{nG_1}^2}}{f_s/2} \int^{f_s/OSR} |NTF_{G_1}|^2\, df && \leftarrow G_1 \\
& + \frac{\overline{v_{np_R}^2}}{f_s/2} \int^{f_s/OSR} \left|NTF_{p_R}\right|^2 df + \frac{\overline{v_{np_I}^2}}{f_s/2} \int^{f_s/OSR} \left|NTF_{p_I}\right|^2 df && \leftarrow z_{cmplx} \\
& + \frac{\overline{v_{nQ}^2}}{f_s/2} \int^{f_s/OSR} |NTF|^2\, df && \leftarrow NTF \qquad (4.8)
\end{aligned}
$$

After substituting for the sampling frequency, f_s, and for the *OSR*, the power transfer functions were integrated in Mathematica [9]. The total output noise power is given by Eq. (4.9):

$$\begin{aligned}
\overline{v_n^2} = {} & \overline{v_{nC_1}^2}\left(7.2 \times 10^{-2}\right) && \leftarrow C_1 \\
& + \overline{v_{nC_{2R}}^2}\left(2.1 \times 10^{-2}\right) + \overline{v_{nC_{2I}}^2}\left(1.0 \times 10^{-1}\right) && \leftarrow C_2 \\
& + \overline{v_{nA_{1R}}^2}\left(4.0 \times 10^{-3}\right) + \overline{v_{nA_{1I}}^2}\left(2.7 \times 10^{-2}\right) && \leftarrow A_1 \\
& + \overline{v_{nA_2}^2}\left(2.0 \times 10^{-4}\right) + && \leftarrow A_2 \\
& + \overline{v_{nA_3}^2}\left(4.0 \times 10^{-4}\right) + && \leftarrow A_3 \\
& + \overline{v_{nF_{1R}}^2}\left(3.0 \times 10^{-3}\right) + \overline{v_{nF_{1I}}^2}\left(2.2 \times 10^{-2}\right) && \leftarrow F_1 \\
& + \overline{v_{nF_{2R}}^2}\left(1.0 \times 10^{-4}\right) + \overline{v_{nF_{1I}}^2}\left(3.0 \times 10^{-4}\right) && \leftarrow F_2 \\
& + \overline{v_{nF_{34R}}^2}\left(7.8 \times 10^{-6}\right) + \overline{v_{nF_{34I}}^2}\left(4.0 \times 10^{-5}\right) && \leftarrow F_{34} \\
& + \overline{v_{nB_{1R}}^2}\left(3.2 \times 10^{-4}\right) + \overline{v_{nB_{1I}}^2}\left(1.3 \times 10^{-3}\right) && \leftarrow B_1 \\
& + \overline{v_{nB_{23R}}^2}\left(1.1 \times 10^{-4}\right) + \overline{v_{nB_{23I}}^2}\left(3.7 \times 10^{-4}\right) && \leftarrow B_{23} \\
& + \overline{v_{nB_{3R}}^2}\left(1.1 \times 10^{-4}\right) + \overline{v_{nB_{3I}}^2}\left(3.7 \times 10^{-4}\right) && \leftarrow B_3 \\
& + \overline{v_{nG_1}^2}\left(3.7 \times 10^{-6}\right) + && \leftarrow G_1 \\
& + \overline{v_{np_R}^2}\left(1.7 \times 10^{-4}\right) + \overline{v_{np_I}^2}\left(3.7 \times 10^{-3}\right) && \leftarrow z_{cmplx} \\
& + \overline{v_{nQ}^2}\left(2.3 \times 10^{-6}\right) + && \leftarrow NTF
\end{aligned} \tag{4.9}$$

In order to simplify the noise analysis, the noise terms with insignificant contribution to the total noise in (4.9) can be dropped. The total noise power is now approximately given by:

$$\begin{aligned}
\overline{v_n^2} = {} & \overline{v_{nC_1}^2}\left(7.2 \times 10^{-2}\right) \\
& + \overline{v_{nC_{2R}}^2}\left(2.1 \times 10^{-2}\right) + \overline{v_{nC_{2I}}^2}\left(1.0 \times 10^{-1}\right) \\
& + \overline{v_{nA_{1R}}^2}\left(4.0 \times 10^{-3}\right) + \overline{v_{nA_{1I}}^2}\left(2.7 \times 10^{-2}\right) \\
& + \overline{v_{nF_{1R}}^2}\left(3.0 \times 10^{-3}\right) + \overline{v_{nF_{1I}}^2}\left(2.2 \times 10^{-2}\right)
\end{aligned} \tag{4.10}$$

The first three terms in the equation represent the noise contribution of the first stage, and the remaining terms represent the noise contribution of the second stage of the modulator.

The next step is to substitute the PSDs for the noise sources. The mean-square value of the input-referred noise voltage of an SC integrator is given by:

$$\overline{v_{ni}^2} = \left(\frac{kT}{C_s}\right)\frac{2x+1}{x+1} \tag{4.11}$$

The input-referred noise (4.11) does not include any noise contribution from the opamp. The opamp thermal noise can be modeled by two noise sources [6], one at its input with a mean-square value of:

$$\overline{v_{ni_{OP}}^2} = \left(\frac{4}{3}\frac{kT}{C_s}\right)\frac{1}{x+1} \tag{4.12}$$

and another at its output with a mean-square value of:

$$\overline{v_{no_{OP}}^2} = \left(\frac{4}{3}\frac{kT}{C_L}\right) \tag{4.13}$$

where C_{L} is the effective load capacitance of the opamp, $x = 2R_{ON}g_m \cdot R_{ON}$ is the switch on-resistance, and g_m is the transconductance of the input MOSFET of the opamp. For the case $x \to \infty$, the total input-referred noise of an integrator is dominated by the noise generated by the SC switches and is equal to $2kT/C_s$.

The second noise term in Table 4.3 models the opamp input-referred noise power,[2] which is stored at the input capacitor branches at the first stage integrator.

The effective load capacitance, C_{L1}, for the first stage is given by (Table 4.4)

$$\begin{aligned} C_{L1} &= C_{S2}\left[1+\frac{A_{1I}}{A_{1R}}\right] + C_{S1}\left[\frac{1+\frac{C_{2R}+C_{2I}}{C_1}}{1+C_1+C_{2R}+C_{2I}}\right] \\ &= 1.413C_{S1} + 3.60C_{S2} \end{aligned} \tag{4.14}$$

[2] For an integrator with several SC input branches, the thermal noise due to switches referred to input branch C_{1a} is given by:

$$\frac{kT}{C_{1a}}\left(\frac{2x+1}{x+1}\right)\left(1+\frac{C_{1b}}{C_{1a}}+\frac{C_{1c}}{C_{1a}}+\cdots\right),$$

However, the opamp input noise referred to the input-branch is given by:

$$\left(\frac{4}{3}\right)\frac{kT}{C_{1a}}\left(\frac{1}{x+\frac{C_{1a}+C_{1b}+\ldots}{C_{1a}}}\right)\left(1+\frac{C_{1b}}{C_{1a}}+\frac{C_{1c}}{C_{1a}}+\ldots\right)^2$$

The equation for opamp noise has been derived assuming that all the SC branches have identical time constants. The modified equation reflects the correlated noise injected at the input branches of the integrator.

Table 4.3 PSDs for the noise sources referred to the sampling capacitor of the first stage of the modulator

PSD term	
$\overline{v_{nC_1}^2}$	$\frac{kT}{C_{S1}}\left(\frac{2x+1}{x+1}\right)\left[1+\frac{C_{2R}+C_{2I}}{C_1}\right]$ ← *Switch noises*
	$+\frac{4}{3}\frac{kT}{C_{S1}}\left(\frac{1}{x+\frac{C_{2R}+C_{2I}+C_1}{C_1}}\right)\left[1+\frac{C_{2R}+C_{2I}}{C_1}\right]^2$ ← *Opamp input noise*

Table 4.4 PSDs for the noise sources referred to the sampling capacitor of the second stage of the modulator

PSD term	
$\overline{v_{nA_{1R}}^2}$	$\frac{kT}{C_{S2}}\left(\frac{2x+1}{x+1}\right)\left[1+\frac{A_{1I}+F_{1R}+F_{1I}}{C_1}\right]$ ← *Switch noises*
	$+\frac{4}{3}\frac{kT}{C_{S1}}\left(\frac{1}{x+\frac{A_{1R}+A_{1I}+F_{1R}+F_{1I}}{A_{1R}}}\right)\left[1+\frac{A_{1I}}{A_{1R}}\right]^2$ ← *Opamp input noise, stage two*
	$+\frac{4}{3}\frac{kT}{C_{L1}}\left[1+\frac{A_{1I}}{A_{1R}}\right]^2$ ← *Opamp output noise, stage one*

For this design, a value of $x = 1$ was selected. Substituting for the PSDs and the coefficients in (4.9), the resulting noise contribution of the first stage of the modulator is:

$$\begin{aligned} v_{n,stage1} &= \frac{kT}{C_{S1}}(0.29)+\frac{kT}{C_{S1}}(0.19) \\ &= \frac{kT}{C_{S1}}(0.49) \end{aligned} \tag{4.15}$$

The noise contribution of the second stage of the modulator is:

$$v_{n,\ stage2} = \frac{kT}{C_{S2}}(0.04)+\frac{kT}{C_{S2}}(0.03)+\frac{kT}{1.413\ C_{S1}+3.60C_{S2}}(0.069) \tag{4.16}$$

For a maximum input signal power of –6 dB and a 12-bit performance, the total noise power, including quantization noise, thermal noise, external noise sources, etc., is $10^{(-6-74)/10}\text{V}^2$=(100 μV)^2. If 65% of the noise power is assigned to thermal noise, the total permissible noise power comes out to be (80.6 μV)^2. Assigning 50% of this noise power, (61.5 μV)^2, to the first stage, and 30%, (44.2 μV)^2, to the second stage of the modulator gives the values for the sampling capacitors in the first stage and the second stage of the modulator.

Table 4.5 Stage capacitor sizes and spreads

	Integration capacitors	Feed-in capacitors				Capacitor spreads
Stage 1	1.878 pF	C_{C1}	$= 642.8\,fF,$			5.4
		C_{C2R}	$= 348\,fF,$	C_{C2I}	$= 771.5\,fF$	
Stage 2	850 fF	C_{A1R}	$= 240.55\,fF,$	C_{A1I}	$= 626.11\,fF,$	17.25
		C_{F1R}	$= 207.23\,fF,$	C_{F1I}	$= 558.79\,fF,$	
		C_{Cc}	$= 49.72\,fF,$	C_{Cd}	$= 286.36\,fF,$	
Stage 3	1 pF	C_{A2}	$= 277.8\,fF,$	C_{B1R}	$= 242.8\,fF,$	39
		C_{B1I}	$= 490.9\,fF,$	C_{F2R}	$= 144\,fF,$	
		C_{Cc}	$= 49.72\,fF,$	C_{Cd}	$= 286.36\,fF,$	
Stage 4	250 fF	C_{A3}	$= 375.0\,fF,$	C_{B2B3R}	$= 288.7\,fF,$	7
		C_{B2B3I}	$= 512.3\,fF,$	C_{B3R}	$= 233.25\,fF,$	
		C_{B3I}	$= 471.55\,fF,$	C_{F3F4R}	$= 73.8\,fF,$	
		C_{F3F4I}	$= 167.32\,fF,$	C_{F3R}	$= 73.8\,fF,$	
		C_{F3I}	$= 167.32\,fF,$			

$$\frac{kT}{C_{S1}}(0.496) = (61.5\mu V)^2$$

$$C_{S1} = 7\ \ 535fF$$

$$\frac{kT}{C_{S2}}(0.07) + \frac{kT}{1.413 \times 543fF + 3.60\,C_{S2}}(0.069) = (44.20\mu V)^2$$

$$C_{S2} = 172fF$$

Due to some process restrictions on the smallest capacitor dimensions that can be drawn, the actual capacitor values used in the implementation are slightly bigger than the sizes given by the noise requirements. The final capacitor sizes used to realize the modulator are listed in Table 4.5.

The impact of thermal noise on the SNR of the ΔΣ modulator was simulated by adding noise sources at the inputs of each coefficient in the behavioral model. Figure 4.23 depicts the model used to simulate the effect of switch thermal noises on the modulator.

4.4.2 Clock-Jitter

Due to the wide bandwidth of DTV signals, about 6–8 MHz, clock jitter will have a significant impact on the SNR of the ADC. Assuming the clock jitter-induced error can be modeled as white noise, with uniform power spectral density from *0* to $f_s/2$ and a total power of [8]:

$$\sigma_{\Delta v}^2 = \frac{(A\omega_{IN})^2}{2}\sigma_{\Delta t}^2 \tag{4.17}$$

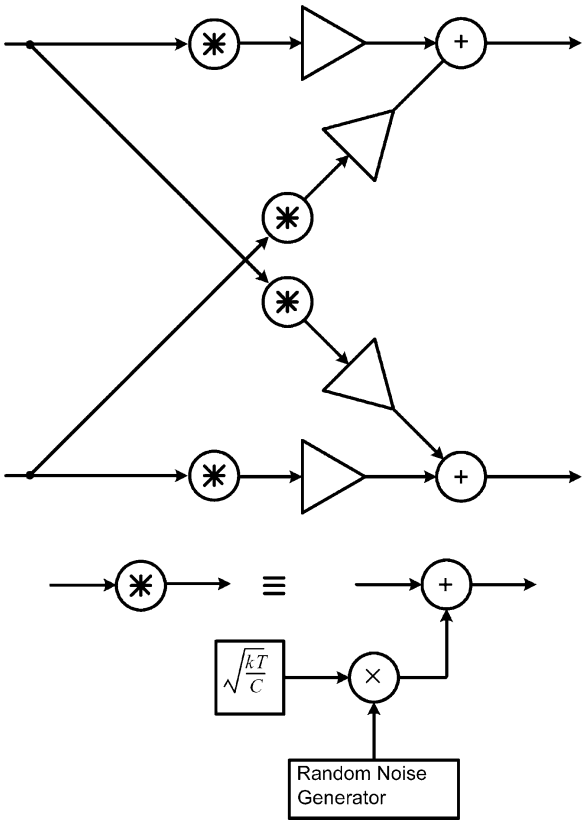


Fig. 4.23 Noise sources to model switch thermal noises in a complex coefficient

The in-band noise power reduced by the oversampling ratio is given by:

$$P_{e,in} = \frac{\sigma_{\Delta v}^2}{OSR} = \frac{(A\omega_{IN})^2}{2OSR}\sigma_{\Delta t}^2 \tag{4.18}$$

The signal-to-noise ratio due to jitter in the sampling clock can be expressed as:

$$SNR_{jiter} = \frac{OSR}{\omega_{IN}^2}\frac{1}{\sigma_{\Delta t}^2} \tag{4.19}$$

From (4.19), for a signal bandwidth of 8 MHz, SNR_{jiter}>80 dB, and OSR of 16, the rms value of the clock jitter should be less than 8 psec. This jitter requirement is severe and, at the targeted sampling frequency of 128 MHz, clock jitter may become the limiting factor for the SNR of the ADC.

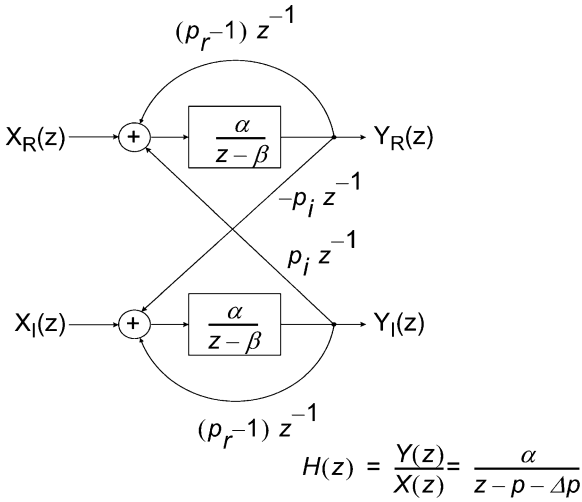


Fig. 4.24 Complex -integrator realized with finite dc gain amplifiers

4.4.3 Opamp Nonidealities

4.4.3.1 Opamp Finite DC Gain

The behavioral model uses the αβγ representation [9] to model the effect of the finite dc gain in a practical SC integrator implementation. Using the αβγ representation, the output of a complex SC integrator (see Fig. 4.24), can be expressed as:

$$H(z) = \frac{Y(z)}{X(z)} + = \frac{\alpha}{z - \alpha p + (\alpha - \beta)} \tag{4.20}$$

Assuming α and β can be modeled as:

$$\begin{aligned} \alpha &= 1 + \Delta\alpha \\ \beta &= 1 + \Delta\beta \end{aligned} \tag{4.21}$$

where α is the gain-error, and β is the frequency error introduced by the finite dc gain of the opamp. These errors modify the transfer function of the complex integrator to

$$H(z) = \frac{Y(z)}{X(z)} = \frac{\alpha}{z - p - \Delta p} \tag{4.22}$$

$\Delta p = p\Delta\alpha - \Delta\alpha + \Delta\beta$ represents the frequency-error introduced in the complex pole by the finite dc gain of the opamp.

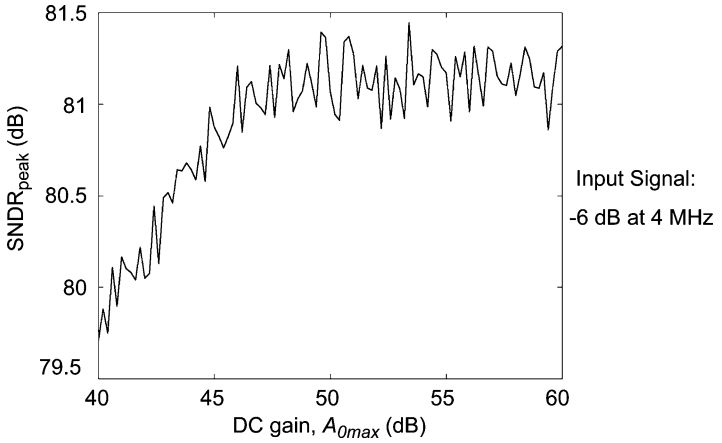


Fig. 4.25 Simulated $SNDR_{peak}$ versus maximum dc gain A_{0max} of the opamps in the experimental ΔΣ modulator

Behavioral simulations were performed to determine the SNDR degradation due to finite dc gains of the opamps. The fourth-order ΔΣ modulator was simulated for various maximum dc gains, A_{0max}, with an input signal of amplitude –6 dB and a frequency of 8 MHz. Figure 4.25 shows the corresponding $SNDR_{peak}$ versus A_{0max}. The modulator shows an SNR degradation of less than 2 dB for an opamp dc gain variation from 30 dB to 60 dB. However, to ensure that there is not a significant SNR loss due to opamp gain nonlinearity, a value of 60 dB for the dc gain is chosen.

4.4.3.2 Unity-Gain Frequency and Slew Rate

Once the capacitor sizes are selected, it is possible to estimate the unity-gain frequency and slew current requirements of the opamps used to realize the integrators in the modulator. Assuming 25% of the half-clock cycle time period is available for slewing, the slew current requirement for an opamp in '*stage i*' can be estimated as:

$$\begin{aligned} I_{SLEWi} &= SRC_{Li} \\ &= \frac{100}{22}\frac{2}{1}128MHz \times 1\ V\, C_{Li} \\ &= 1.024 \times 10^9 C_{Li} \end{aligned} \tag{4.23}$$

Where C_{Li} is the capacitance load for opamp in '*stage i*'.

Table 4.6 Opamp open-loop requirements

Opamp	C_L [pF]		β		f_{UGBW} [GHz]	G_m [mS]		I_{SLEW} (μA)	I_{SETT} (μA)
	Φ_1	Φ_2	Φ_1	Φ_2		Φ_1	Φ_2		
Stage 1[a]	2.82	1.12	1.0	0.4	1.88	13.36	13	573	650
Stage 2[b]	0.87	0.28	0.3	1.0	2.50	13.65	1.35	446	650
Stage 3[a]	0.37	0.58	1.0	0.42	1.79	1.77	6.74	301	337
Stage 4[b]	0.19	3.79	1.0	0.24	3.13	9.0	3.6	985	450

[a]Φ_2 is the holding phase, and Φ_1 is the integrating phase
[b]Φ_1 is the holding phase, and Φ_2 is the integrating phase

Assuming that the opamp has a single dominant pole and is not slewing, then the response of the integrator to a step input can be described as an exponential with a time constant 'τ' given by [10]:

$$\tau = \frac{C_L}{\beta g_m} \tag{4.24}$$

For an integrator to settle to resolution of N_B-bits in the settling time 't_{sett}', the time constant 'τ' is given by:

$$\tau = \frac{t_{sett}}{In(2^{N_B})} \tag{4.25}$$

Assuming that for the proposed modulator 65% of the half-period is available for integrator settling, and the first integrator has to settle to a resolution of 12-bits, then from (4.24) and (4.25) we have:

$$f_{UGBW} = \frac{g_m}{2\pi C_L} = \frac{7.52 \times 10^8}{\beta} \tag{4.26}$$

Equation (1.26) was used to calculate the unity-gain frequency (f_{UGBW}) requirements for the four opamps. The calculated values for f_{UGBW} are shown in Table 4.6. However, due to the noise-shaping in the ΔΣ modulator, it should be possible to relax the settling requirements and hence required f_{UGBW} for the integrators in the subsequent stages. From (4.26) the loop-gain bandwidth ($f_{LGBW} = f_{UGBW} \times \beta$) for the opamp is 752 MHz.

The opamp input device current required to realize the transconducatnce (g_m) shown in Table 4.6 can be estimated from:

$$I_{SETT} = \frac{g_m V_{ov}}{2} \tag{4.27}$$

The calculated values for I_{SETT} for an overdrive voltage (V_{ov}) of 0.1 V are shown in Table 4.6.

4.4.4 Switch On-Resistances

In an SC implementation of the modulator, the switches are implemented with NMOS and PMOS devices. The finite switch-on resistance and other non-ideal behavior of these devices can degrade the performance of the integrators and of the modulator as a whole.

It is possible to decide on the type of the switch, PMOS, NMOS, or CMOS transmission gate, on the basis of the node to which the switch is coupled. For example, switches coupled to the summing junction of the integrator have one side either connected to analog ground or to the summing junction of the opamp. With the switch arrangement shown in Fig. 4.17, and with the choice of low-voltage for analog ground, it should be possible to use NMOS devices for the summing junction switches. The switches coupled to the input signal or the output of the opamp have full signal swing across them and, as a result, it may be necessary to use CMOS transmission gates for these switches. To minimize parasitics, minimum gate length devices will be chosen. The aspect ratio W/L of the devices will also be selected so that the time constant $T_{ON} = (R_{ON}C)$ of the switch satisfies the equation [11]:

$$T_{ON} < \frac{mT}{7} \tag{4.28}$$

where mT is the time-period available for the charging of the capacitor C.

References

1. Schreier, R., Temes, G.C.: Understanding Delta-Sigma Data Converters. Wiley-IEEE Press, New York (2004) ISBN 0-471-46585-2
2. Jantzi, S.A., Martin, K.W., Sedra, A.S.: The effects of mismatch in complex bandpass ΔΣ modulators. IEEE International Symposium on Circuits and Systems, vol. 1, pp. 227–230, 12–15 May 1996
3. The Math Works, Inc., *Simulink*, Version 6.4, The Math Works, Inc., Natick, Massachusets
4. Kenney, J.G., Carley, L.R.: CLANS: a high-level synthesis tool for high resolution data converters. ICCAD Digest of Technical Papers, pp. 496–499, November 1988
5. Haigh, D.G., Singh, B.: A switching scheme for switched capacitor filters which reduces the effect of parasitic capacitances associated with switch control terminal. Proceedings of the IEEE International Symposium on Circuits and Systems, vol. 2, pp. 586–589, June 1983
6. Schreier, R., Silva, J., Steensgaard, J., Temes, G.C.: Design-oriented estimation of thermal noise in switched-capacitor circuits. IEEE Trans. Circuits Syst. **15**(11), 2358–2368 (2005)
7. Research, W.: Inc., *Mathematica*, Version 6.0, Wolfram Research, Champaign, IL.
8. Boser, B.E., Wooley, B.A.: The design of sigma-delta modulation analog-to-digital converters. IEEE J. Solid-State Circuits **26**(12), 1746–1756 (1991)

9. Ki, W.-H., Temes, G.C.: Offset-compensated switched-capacitor integrators. Proceedings of the IEEE International Symposium on Circuits and Systems, pp. 2829–2832, May 1990
10. Temes, G.C.: Finite amplifier gain and bandwidth effects in switched-capacitor filters. IEEE J. Solid-State Circuits **15**(3), 358–361 (1980)
11. Gregorian, R., Temes, G.C.: Analog MOS Integrated Circuits for Signal Processing. Wiley-Interscience, New York (1986) ISBN 978-0471097976

Chapter 5
Integrated Circuit Implementation

The previous chapter discussed the architecture and system level considerations in the design of the proposed fourth-order complex ΔΣ modulator. The required specifications for each building block were also discussed in that chapter. This chapter discusses the implementation of each of these blocks in a 0.18 μm CMOS technology. Due to a high sampling clock frequency and the mixed-signal nature of the ADC, special care has to be taken to minimize the cross-talk of digital noise into the sensitive analog nodes. In Chap. 4, the impact of mismatch on the SNDR and IMR of the ADC was discussed. In the layout of the ADC, special attention must be paid to minimizing the mismatch between the real and the quadrature channels. The chapter discusses the layout considerations that were taken into account and the techniques that were followed during the layout of the proposed ΔΣ modulator.

5.1 The Complete Fourth-Order SC-Modulator

The discrete nature of the proposed ΔΣ modulator lends itself easily to realization with switched-capacitor (SC) circuits. Due to the advantages of higher power supply rejection, reduced clock feed-through and charge injection errors, rejection of even-order non-linearities, and increased dynamic range, a fully-differential configuration was chosen for the implementation of the SC circuits. The single-ended representation of the SC implementation of the ΔΣ modulator presented in Chap. 4 is shown again in Fig. 5.1.

The modulator is clocked by nonoverlapping two phases, ϕ_1 and ϕ_2, of the clock. To a first order, the charge-injection by the MOS switches is canceled by the fully-differential implementation of the modulator. The modulator uses bottom-plate sampling [1] to suppress signal-dependent charge injection. During ϕ_1, all of the switches labeled 1 are close, while those labeled 2 are open. Similarly, during ϕ_2, all of the switches labeled 2 are closed, while switches labeled 1 open. The switches labeled 1_e and 2_e are closed by early versions of ϕ_1 and ϕ_2. The output of each channel goes to a 4-bit quantizer. In addition to fifteen comparators, two additional

B. Pandita, *Oversampling A/D Converters with Improved Signal Transfer Functions*, Analog Circuits and Signal Processing, DOI 10.1007/978-1-4614-0275-6_5,

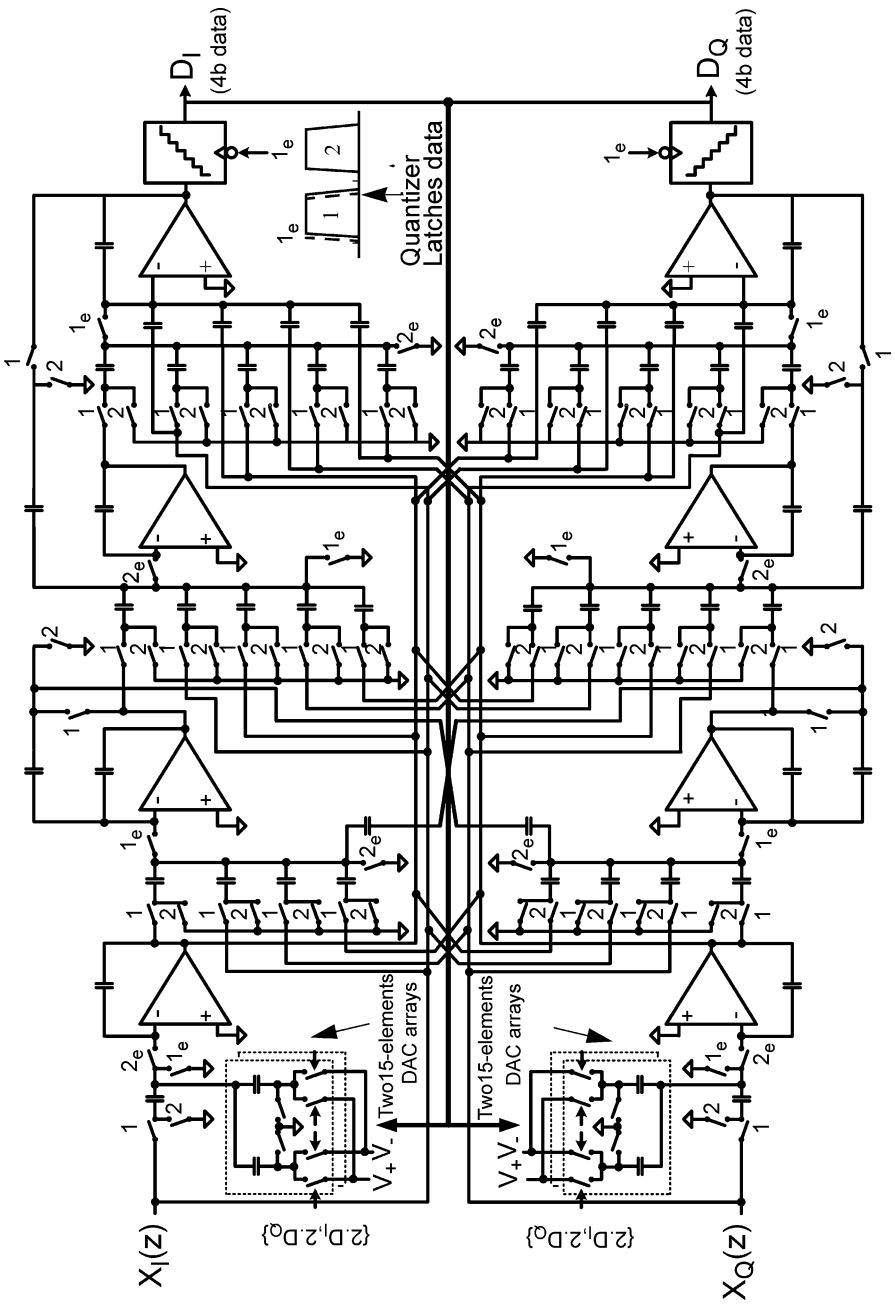


Fig. 5.1 Single-ended representation of the SC implementation of the complex ΔΣ modulator

comparators have been added to the quantizers to indicate the stability status of the modulator. The comparators are ac-coupled and comprise a two-stage preamplifier-latch structure. The15-bit thermometer code of the quantizer drives the SC DAC during ϕ_2.

5.2 Clock Generator

Figure 5.2 shows the logic circuit diagram of the clock generator used to generate the two phases of the nonoverlapping clock for the proposed ΔΣ modulator. The signal *CLK* shown in the diagram is an external input master-clock fed to the clock generator. The clock generator comprises two cross-coupled NOR gates forming an R-S flip-flop. One NOR gate receives the master-clock after an inversion, whereas, in the case of the second NOR gate, the input clock is delayed through a transmission-gate, TG, to compensate for the inverter delay. The NOR gates followed by the additional inverters generate the nonoverlapping clock phases, ϕ_1 and ϕ_2, respectively. As mentioned in the previous section, the modulator uses early versions of ϕ_1 and ϕ_2 to reduce the effects of signal-dependent charge injection.

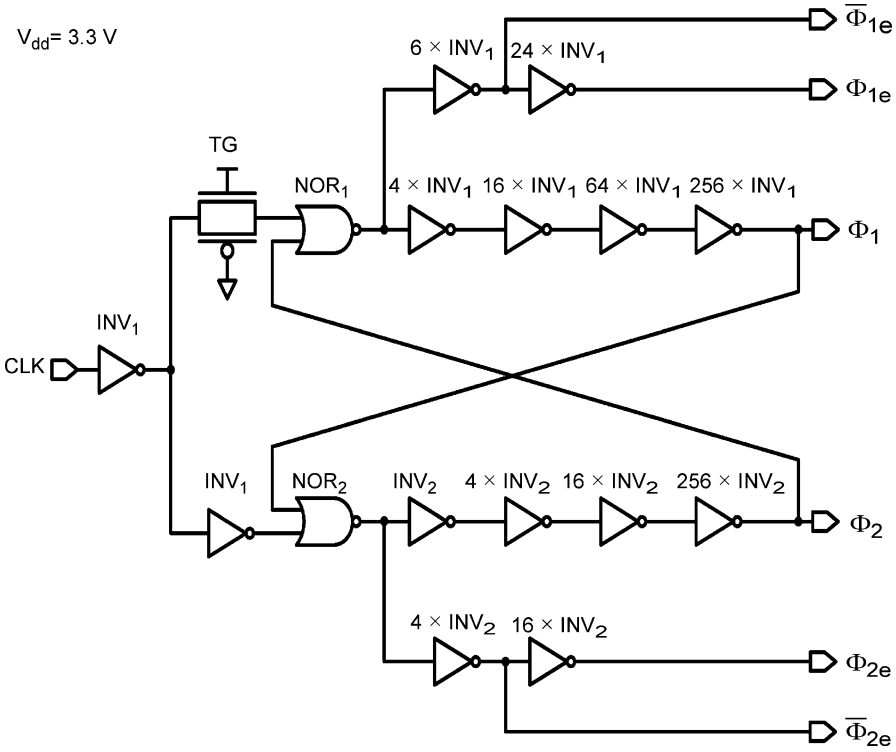


Fig. 5.2 Two-phase nonoverlapping clock generator

Table 5.1 Device sizes in the clock generator[a]

Gate	PMOS	NMOS
INV_1	6.2/0.30	1.7/0.35
INV_2	5.6/0.30	1.53/0.35
NOR_1	16/0.30	4/0.35
NOR_2	10.5/0.30	2.25/0.35
TG	3.5/0.30	1/0.30

[a] W/L (μm/μm)

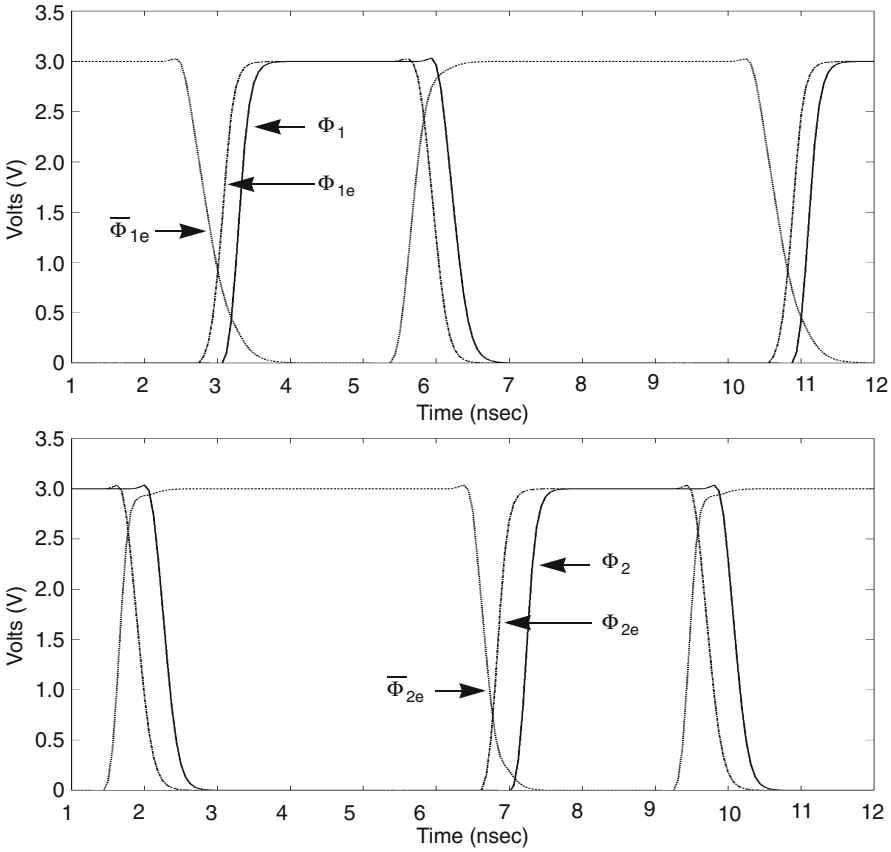


Fig. 5.3 Clock signals for the two phases, their early versions, and the inverted early phases

The early clock versions, ϕ_{1e} and ϕ_{2e}, are generated directly from the outputs of the NOR gates. The logic gates have been sized in order to make the rise-times and fall-times of the phases equal. Device sizes for each gate are given in Table 5.1.

The switches in the modulator are 3.3 V thick-oxide NMOS transistors, which are closed when the controlling clocks are high. Figure 5.3 shows the simulation output of the clock generator; the clock phases are loaded with capacitive loads equal to the gate-capacitances the phases are driving.

5.3 Sampling Switches

In the SC implementation of the proposed ΔΣ modulator, the input common-mode of the opamps has been set approximately at 0.5 V and the output common-mode at 0.9 V. The positive and negative reference voltages for the DAC have been set at 0.4 V and 1.4 V respectively. The DAC feedback switches have been realized with CMOS switches with regular MOS devices. To avoid the need for transmission-gates or clock boosting, the remaining switches in the modulator have been implemented with 3.3 V thick-oxide NMOS transistors. Depending upon the value of the capacitor load, the switches are sized so that the charging time-constant satisfies an accuracy condition of 12-bits.

5.4 Operational Amplifier

5.4.1 Main Stage

The amplifiers used in the integrators are designed to drive the capacitive loads to 12-bit settling in 3.5 ns. The specifications for the amplifiers were derived in Chap. 4. The behavioral simulations in Chap. 4 have demonstrated a negligible SNDR degradation for a maximum opamp dc-gain variation from 30–60 dB. However, a dc-gain of 60 dB was selected to suppress opamp harmonic distortion adequately.

At a power supply of 1.8 V, 60 dB dc-gain can be easily achieved with a single-stage gain-boosted folded-cascode opamp. The folded-cascode opamp shown in Fig. 5.4 is designed with a PMOS differential pair, M_1 and M_2. The swing at the output of the opamp has been maximized by biasing the NMOS current sinks, M_3 and M_4, and M_6 and M_8, and the PMOS current sources, M_9 and M_{10}, and M_{11} and M_{12}, at the edge of the triode region; the drain-source voltage for these transistors has been set approximately at their overdrive voltage. For a power supply of 1.8 V, the differential output swing of the opamp is 2 $V_{p\text{-}p}$. The output common-mode voltage of the opamp has been set at 0.9 V, which is half the supply voltage. The input common-mode of the opamp has been set at approximately 0.5 V, which is a value higher than 0 V, in order to guarantee a minimum positive input common mode voltage under all conditions [2, 3].

Voltages V_{p1}, V_{p2}, V_{n1}, and V_{n2} are set by a separate bias stage, and the voltage V_{cmfb} is set by the common-mode feedback voltage circuit. The NMOS cascode transistors, M_3 and M_6, and the PMOS cascode transistors, M_{10} and M_{12}, are gain-boosted with additional fully-differential amplifiers.

The input stage transistors are designed to achieve the desired unity-gain frequency. The NMOS transistors, M_3 and M_6, and the PMOS transistors, M_{10} and M_{12}, have been designed with minimal lengths ($L = 0.18\mu m$) in order to place the nondominant pole of the opamp at a high frequency. For transistors M_9, M_{11},

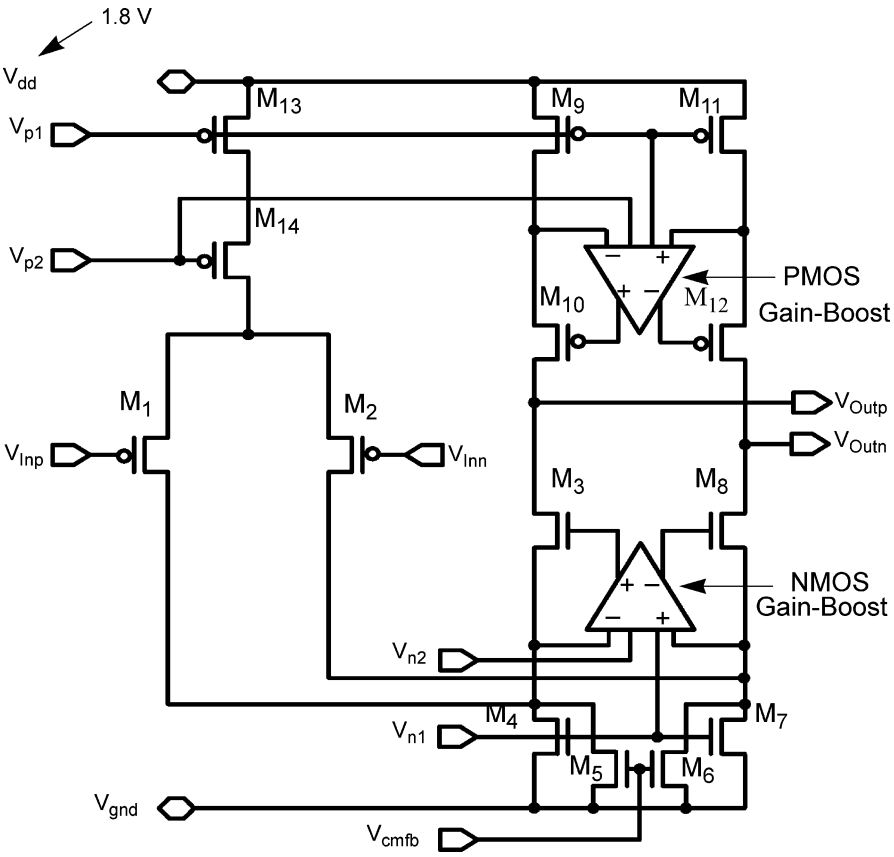


Fig. 5.4 Operational amplifier main stage

M_4, M_5, M_7, and M_8 longer channel lengths have been chosen in order to achieve better matching.

Figure 5.5 shows the closed loop frequency-response simulations of the overall amplifier for the first stage of the modulator. The amplifier achieves a loop-gain of 56 dB, a loop-gain bandwidth of 750 MHz, and a phase margin greater than 75°.

5.4.2 Bias Stage

Each opamp in an integrator has its own local biasing circuit. The input to the biasing circuit is a bias current generated by a master bias current distribution circuit (refer to Fig. 5.6). The master bias current circuit mirrors a current generated off-chip, and the mirrored currents are distributed to local biasing circuits through

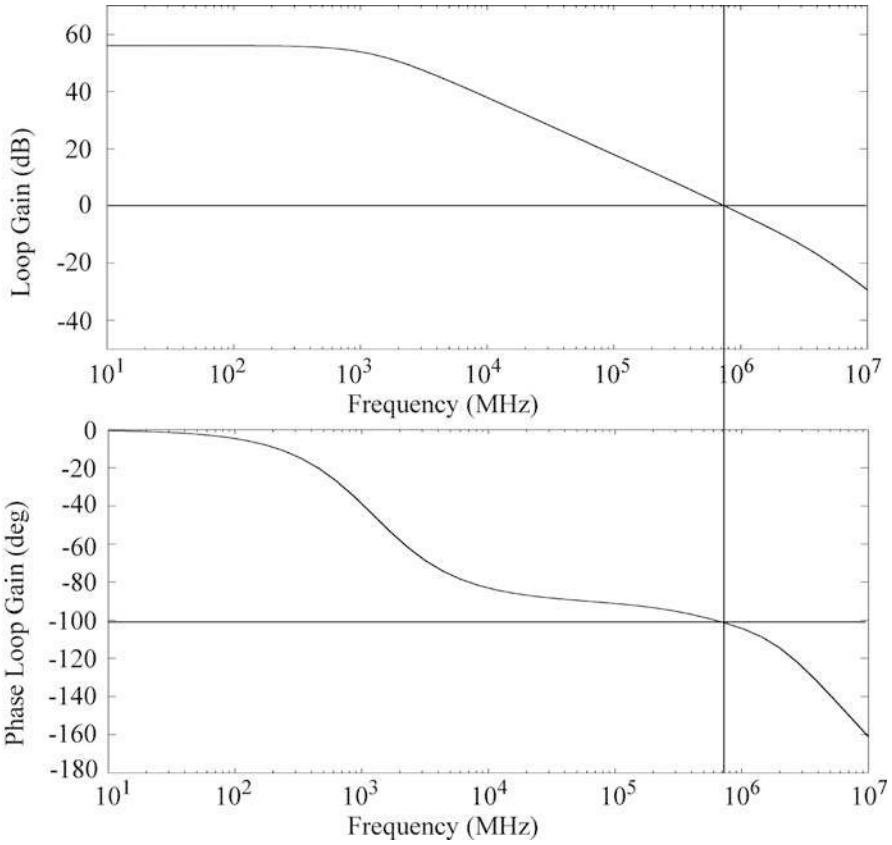


Fig. 5.5 Opamp loop-gain magnitude and phase response – first stage of the modulator

NMOS cascode current- mirroring circuits. It is possible to independently adjust the bias current to each biasing stage through the use of digital trim bits.

The opamp uses high-swing cascode mirrors to set the bias levels (see Fig. 5.7). *Ibias* in the figure is an off-chip bias current input. M_1 and M_2 together with M_3–M_5 form a wide-swing cascode current mirror and set the bias voltages V_{p1} and V_{p2}, of the main opamp. M_3–M_5 form a composite device to bias M_1 at a gate voltage of $V_{tp} + 2V_{ov}$ (V_{tp} is the threshold voltage of the PMOS transistor, and the overdrive voltage V_{ov} has been set at approximately 0.15 V). The drain-source voltage for M_2, and hence for M_9 and M_{11} in Fig. 5.4, is set at the overdrive voltage V_{ov}. Similarly, M_{19} and M_{20}, together with M_{11}–M_{13}, form a wide-swing cascode current mirror to set the bias voltages V_{n1} and V_{n2}. The drain-source voltage for M_{20}, and for M_4 and M_8 in Fig. 5.4, is set at the overdrive voltage V_{ov}. This wide-swing biasing arrangement helps to maximize the voltage swing at the output of the opamp. M_{16} is a diode-connected transistor that sets the input common-mode, V_{comi}, of the opamp.

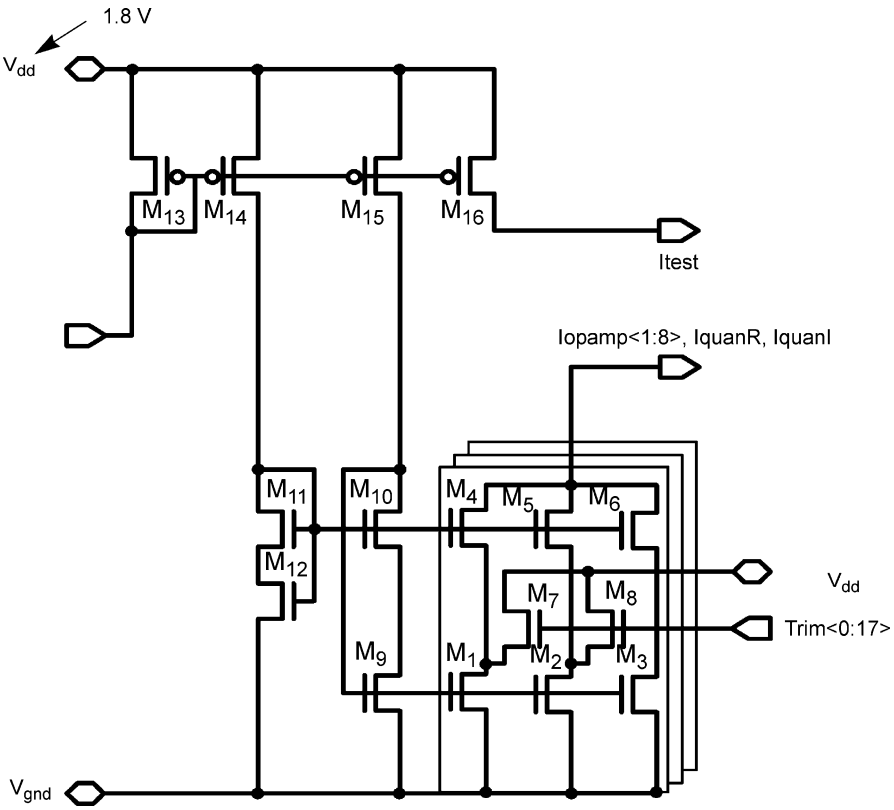


Fig. 5.6 Master bias circuit for the modulator

5.4.3 Gain-Boosting Amplifiers

The gain-boosting amplifiers have been designed with reduced current in order to minimize power dissipation of the complete opamp. The detailed circuit diagram of the NMOS gain-boost amplifier is shown in Fig. 5.8. Since the input to the amplifier is closer to the ground rail, a PMOS input amplifier has been used. The circuit uses a circuit mirror arrangement, M_{17}–M_{19}, in order to make the output CM level of the amplifier equal to the desired reference voltage, V_{n1}. The cascode NMOS devices of the main opamp, M_3 and M_6 in Fig. 5.4, compensate the amplifier. The PMOS gain-boost amplifier, which is shown in Fig. 5.9, is similar to the NMOS gain-boost amplifier Table 5.2.

5.4.4 Device Sizes

Table 5.3 shows the sizes for the devices in the amplifier used in the first stage of the modulator. The opamp used in the second stage of the modulator is identical to the

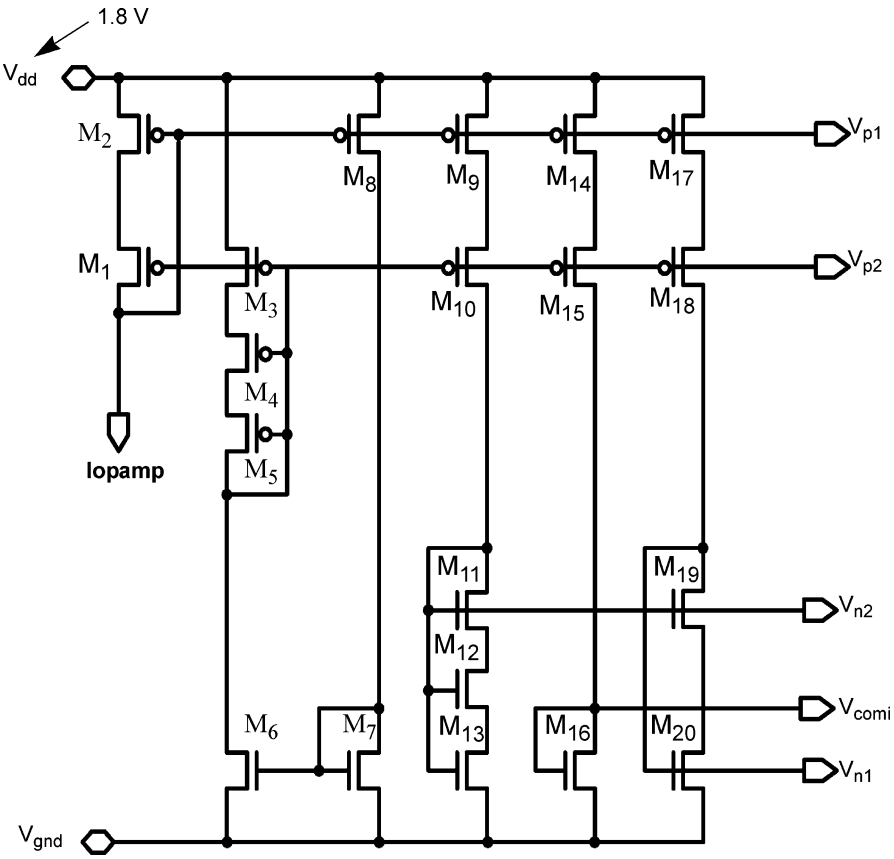


Fig. 5.7 Biasing circuit for the opamp

first-stage amplifier; however, for the third and fourth stages of the modulator, circuit simulations in Spectre [4] show that it is possible to scale the opamp currents by 30% without any adverse impact on the SNDR of the modulator Table 5.4.

5.4.5 SC CMFB Circuit

The opamp output common-mode voltage is controlled by an SC common-mode feedback circuit shown Fig. 5.10 [5]. The output common-mode voltage of the opamp is set by the current flowing through transistors M_5 and M_7, which are shown in Figure 5.4. Capacitors C_1 and C_2, which are not switched, form a voltage divider to sense the common-mode output voltage of the opamp, and after a level-shift set the biasing voltage for the transistors M_5 and M_7. Capacitors C_3 and C_5 provide the necessary level-shift voltage to C_1 and C_2. V_{como}, the desired output common-mode

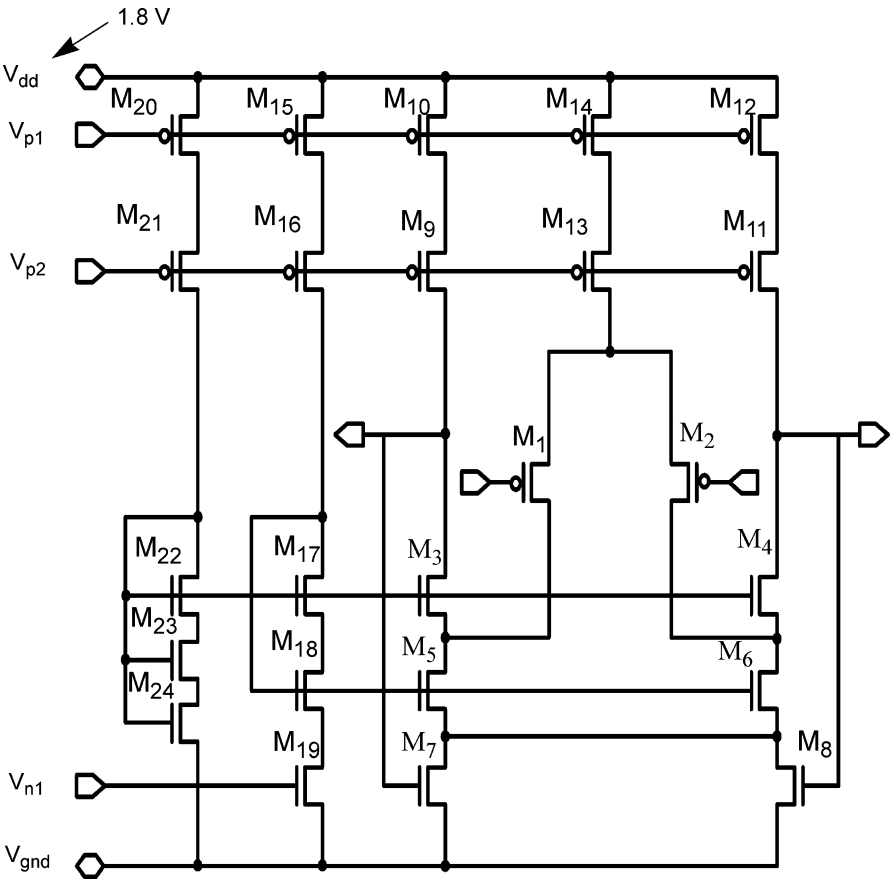


Fig. 5.8 Circuit diagram of the NMOS device gain-boost amplifier

voltage, has been set at 0.9 V, about half the supply voltage. The switches S_1–S_6 in the circuit, which are shown in the Figure 5.10, are 3.3 V thick-oxide NMOS transistors controlled by two nonoverlapping clock phases ϕ_1 and ϕ_2 Table 5.5.

5.5 Quantizers

Each channel of the modulator has a quantizer that produces the 4-bit digital output and the 15 levels that drive the feedback DAC. In the SC implementation of the proposed ΔΣ modulator, the 4-bit quantizers have been realized as 15-level flash ADCs. A resistor ladder generates the threshold voltages for the 15 comparators. The resistor ladder top and bottom are connected to reference voltages of 1.4 V and 0.4 V respectively. The output of the flash ADCs is fed to a bubble-correction logic, which converts the thermometer code to a "1 of 16" code (one-hot encoding). A PLA converts the one-hot code to binary logic.

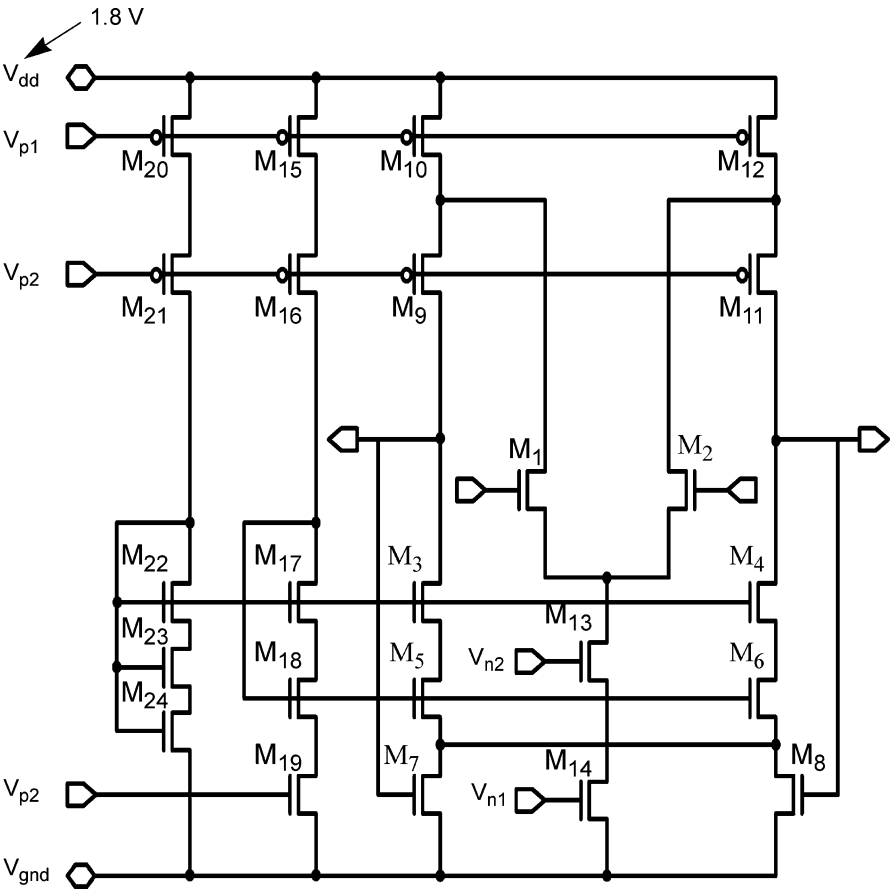


Fig. 5.9 Circuit diagram of the PMOS device gain-boost amplifier

Table 5.2 Master bias device sizes

Component	Size[a]
M_1, M_2	$2 \times 1.0/0.5$
M_3	$6 \times 1.0/0.5$
M_4, M_5	$4 \times 1.0/0.5$
M_6	$12 \times 1.0/0.5$
M_7, M_8	$1 \times 1.0/0.18$
M_9	$6 \times 1/0.50$
M_{10}	$12 \times 1.0/0.18$
M_{11}	$4 \times 10/0.50$
M_{12}	$2 \times 1.0/0.50$
M_{13}, M_{14}, M_{15}	$8 \times 3.0/0.50$
M_{16}	$2 \times 3.0/0.50$

[a] W/L (μm/μm)

Table 5.3 Opamp and bias stage device sizes

Opamp		Bias Stage	
Component	Size[a]	Component	Size[a]
M_1, M_2	104 × 3.0/0.18	M_1	3 × 3.0/0.18
M_9, M_{11}	120 × 3.0/0.35	M_2	4 × 3.0/0.35
M_{13}	240 × 3.0/0.35	M_3, M_4, M_8	2 × 3.0/0.35
M_{10}, M_{12}	120 × 3.0/0.18	M_9	1 × 3.0/0.35
M_{14}	240 × 3.0/0.18	M_5, M_{10}	1 × 3.0/0.35
M_3, M_8	120 × 1.0/0.18	M_{14}, M_{17}	12 × 3.0/0.35
M_4, M_5, M_6, M_7	120 × 1.0/0.50	M_{15}, M_{18}	12 × 3.0/0.18
		M_6, M_7	2 × 1.0/0.70
		M_{11}, M_{12}, M_{13}	1 × 1.0/0.50
		M_{16}	32 × 1.0/0.50
		M_{19}	12 × 1.0/0.18
		M_{20}	12 × 1.0/0.50

[a] W/L (μm/μm)

Table 5.4 NMOS and PMOS gain-booster device sizes

NBoost		PBoost	
Component	Size[a]	Component	Size[a]
M_1, M_2	4 × 3.0/0.18	M_1, M_2	10 × 1.0/0.18
M_3, M_4	6 × 3.0/0.18	M_3, M_4	9 × 1.0/0.18
M_5, M_6, M_7, M_8	12 × 3.0/0.50	M_5, M_6, M_7, M_8	9 × 1.0/0.50
M_9, M_{11}	4 × 3.0/0.18	M_9, M_{11}	3 × 3.0/0.18
M_{10}, M_{12}	4 × 3.0/0.35	M_{10}, M_{12}	6 × 3.0/0.35
M_{13}	8 × 3.0/0.18	M_{13}	9 × 1.0/0.18
M_{14}	8 × 3.0/0.35	M_{14}	9 × 1.0/0.50
M_{15}	2 × 3.0/0.18	M_{15}	1 × 3.0/0.35
M_{16}	2 × 3.0/0.35	M_{16}	1 × 3.0/0.18
M_{17}	3 × 3.0/0.18	M_{17}	3 × 3.0/0.18
M_{18} M_{19}	3 × 3.0/0.50	M_{18}, M_{19}	3 × 3.0/0.50
M_{20}	1 × 3.0/0.35	M_{20}	1 × 3.0/0.35
M_{21}	1 × 3.0/0.18	M_{21}	1 × 3.0/0.18
M_{22}, M_{23}, M_{24}	1 × 3.0/0.50	M_{22}, M_{23}, M_{24}	1 × 1.0/0.50

[a] W/L (μm/μm)

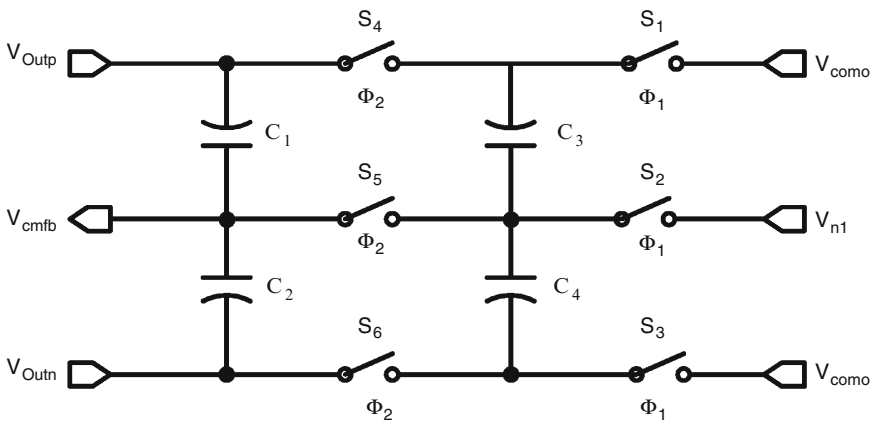


Fig. 5.10 CMFB circuit for the opamp

Table 5.5 Sizes of the switches and capacitors in the CMFB circuit

Component	Size
C_1, C_2	256 fF
C_3, C_4	192 fF
S_1–S_6	$4 \times \frac{1}{0.35} \frac{\mu m}{\mu m}$

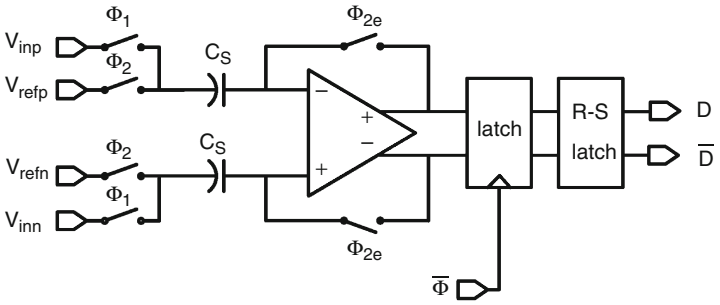


Fig. 5.11 Comparator block diagram

5.5.1 Comparator

For the proposed ΔΣ modulator, each comparator must have an accuracy of 125 mV to meet the resolution requirements of 4-bits. The comparator has been implemented as an ac-coupled preamplifier followed by a regenerative latch. Because of the high-speed requirements, the regenerative latch has been designed with small devices. A sufficiently high-gain pre-amplifier and an input-offset storage scheme ensure that the latch offset does not cause serious quantization errors. An R-S latch holds the comparator output during the reset phase,ϕ_{2e} (refer to Fig. 5.11 for the comparator block diagram). The value of the sampling capacitor has been selected to be 150 fF.

The quantizer operates as follows: During the clock phase ϕ_2, the comparator is in the reset phase, and the sampling capacitors, C_S, sample the reference voltages generated by the resistor ladder. To minimize sampling errors resulting from the charge injection of the switches, the pre-amplifier reset switches are controlled by the early clock phase ϕ_{2e}. The result of the previous comparison is held by the R-S latch. At the rising edge of the clock phase ϕ_1, the sampling capacitors are connected to the modulator channel output, and the pre-amplifier starts amplifying the difference between the channel output and the reference voltages. At the rising edge of $\overline{\phi_{1e}}$, the regeneration latch goes into regeneration, and the output after the delay through the R-S latch is applied to the feedback DAC, during ϕ_2.

Since the residue-offset, that is, the offset divided by the dc gain, of the pre-amplifier remains uncompensated, it is necessary to properly select the dc-gain and device sizes of the pre-amplifier. The pre-amplifier has been designed with a gain of ten. The pre-amplifier has been implemented as a NMOS input differential pair with diode-connected PMOS loads. M_3 and M_4 in the comparator circuit diagram, refer to

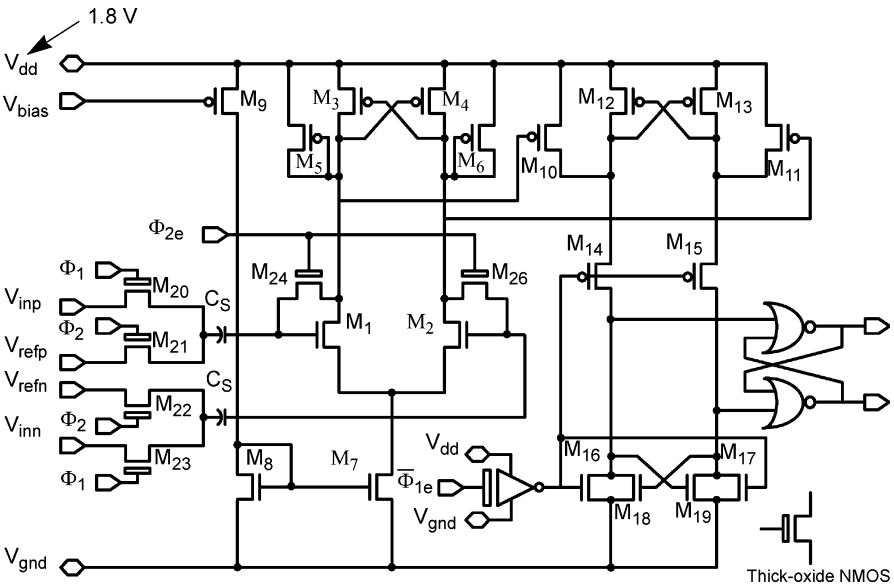


Fig. 5.12 Comparator circuit diagram

Table 5.6 Comparator device sizes

Pre-amplifier		Regenerative latch	
Component	Size[a]	Component	Size[a]
M_1, M_2	3 × 1.0/0.18	M_{10}, M_{11}	3 × 1.0/0.18
M_3, M_4	3 × 1.0/0.18	M_{12}, M_{13}	3 × 1.0/0.18
M_5, M_6	3 × 1.0/0.18	M_{14}, M_{15}	3 × 1.0/0.18
M_7	3 × 1.0/0.18	M_{16}- M_{19}	3 × 1.0/0.18
M_8	3 × 1.0/0.18		
M_9	3 × 1.0/0.18		
M_4, M_5, M_7, M_8	3 × 1.0/0.18		
M_{20}- M_{26}[b]	4 × 1.0/0.35		
C_S	150fF		

[a] MOS device sizes are in μm
[b] Thick-oxide NMOS devices

Table 5.7 Logic-gate device sizes in the comparator

Gate	PMOS[a]	NMOS[a]
NOR	1 × 1.6/0.18	1 × 0.4/0.18
INV[b]	1 × 2.0/0.30	1 × 0.9/0.3

[a] W/L (μm/μm)
[b] Thick-oxide NMOS and PMOS devices

Fig. 5.12, have been introduced in order to decrease the load transconductance, and hence increase the gain of the pre-amplifier. The regenerative latch is based on [6]. The result of Monte Carlo transient simulation of the comparator using circuit simulator Spectre [4] shows that the standard-deviation, σ, of the input-referred offset of the comparator is less than ±10.5 mV (refer Fig. 5.13) (Table 5.6 and 5.7).

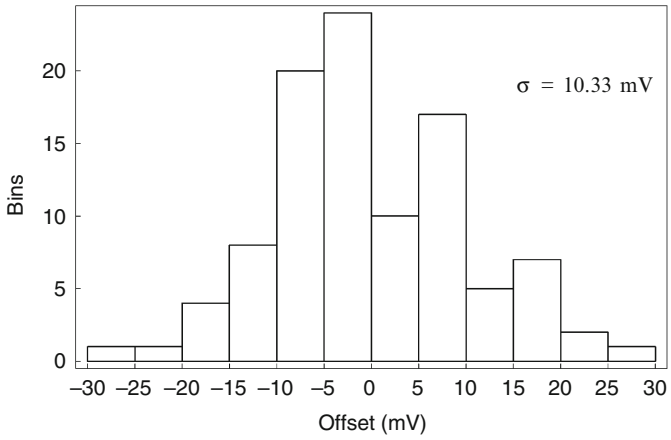


Fig. 5.13 Result of the Monte Carlo transient simulation performed to determine the input-referred offset of the comparator

5.5.2 Resistor Ladder

The resistor ladder for the proposed ΔΣ modulator comprises 30 unit resistor segments with a unit size of R = 24 Ω (see Fig. 5.19). The size of the unit resistor segment was selected to ensure that the largest time constant, formed by the center ladder tap and the capacitor at the input of the comparator, is small enough for the ladder tap voltages to settle to their proper value by the end of the reference-sampling clock phase [7].

5.6 Layout

The proposed ΔΣ modulator was fabricated in a 0.18 μm CMOS process. The modulator occupies a total area of 2.5 mm by 1.8 mm. The micrograph of the chip is shown in Chap. 6. The layout of the ΔΣ modulator is composed of the opamps, the biasing circuitry, switches, capacitors, and quantizers, and other digital logic. During the layout of the modulator, special attention has to be paid to the often conflicting requirements of the aspect ratio and the matching constraints. A symmetrical layout was chosen for the analog and digital blocks in the modulator in a way that was consistent with the fully-differential implementation of the modulator. Fig. 5.14 shows the floor plan of the modulator. The placement of the real and imaginary channels and the four stages in a channel reflect the horizontal and vertical symmetry of the layout. The analog input sampling switches of the firststage are at the left of the layout, and are followed by stages one through four for each channel. The two quantizers are at the right of the channels. The clock input pad and the clock generator have been placed at the right of the layout;

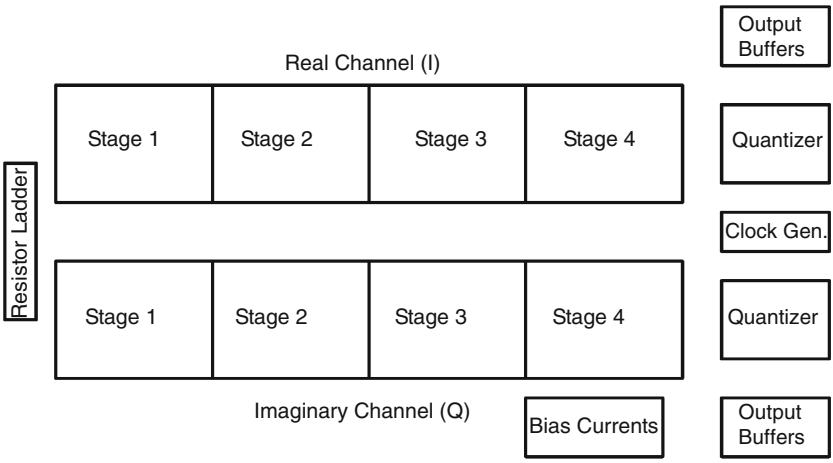


Fig. 5.14 Modulator floor-plan

the direction of the clock phases is opposite to the flow of the analog signal. Special attention has been paid to matching the delays of the different clock phases.

During the layout of the modulator, care was taken to minimize layout mismatches between the nominally-matched analog components and also to reduce parasitic capacitances at the sensitive analog nodes. To minimize noise coupling, digital circuitry has been placed away from the sensitive analog blocks. The clock lines, which are running horizontally along the top and bottom of the layout, have been shielded and placed at a greater distance from the two channels. Vertical buses connect the switches in a stage to the clock lines. Horizontal and vertical buses between the two channels connect the signals between the real and imaginary channels, and also connect the input feed-ins to the integrator stages.

The next important layout aspect after the digital-analog interference consideration of each stage is the layout of the integrators. Fig. 5.15 shows the layout shape for first-stage integrator. The layout shows the opamp, the capacitor arrays, and the analog switches. The layout for the remaining stages of the modulator follows a similar plan. The placement shown in Fig. 5.15 achieves the objective of isolating the switching blocks, e.g., the switches, from the sensitive analog nodes.

5.6.1 Capacitor

Metal-insulator-metal (MIM) capacitors available in the technology were used to realize the various capacitors in the modulator. The matched capacitors are implemented as arrays of unit capacitors and a nonunit capacitor per array having an equal area-to-periphery ratio. A Mathematica [8] program calculates the width and length needed for each nonunit capacitor to maintain the proper perimeter-to-area ratio.

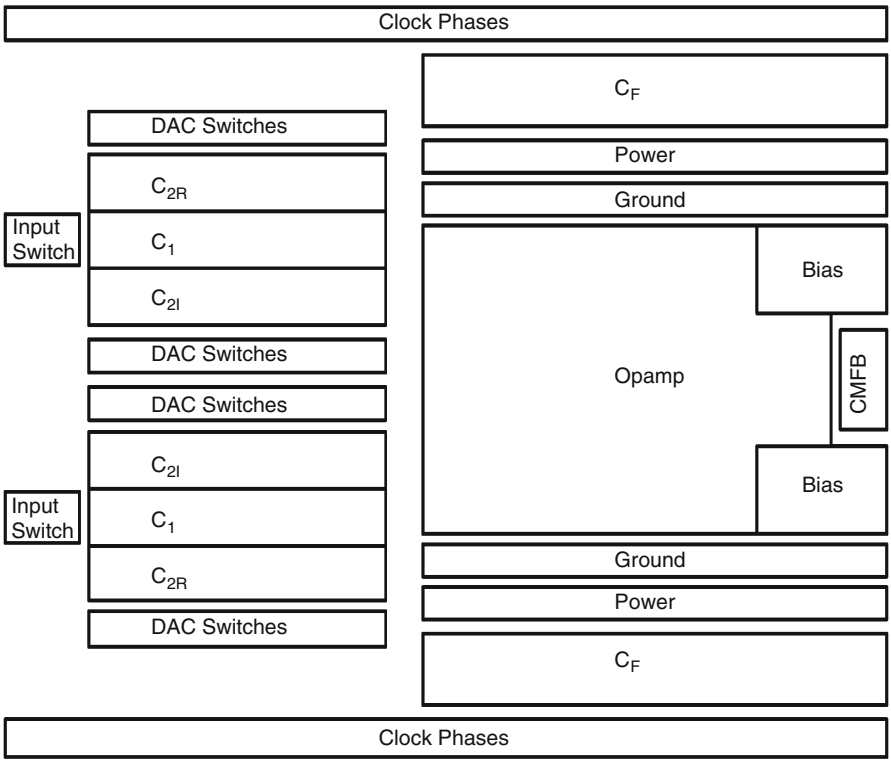


Fig. 5.15 Layout plan for the first stage of the modulator channel

To minimize capacitor mismatches due to etch variations, the capacitor arrays are surrounded with dummy capacitors, which are connected to the power supply. The capacitor interconnects are properly balanced to minimize mismatches caused by the parasitics introduced by the leads. The capacitor bottom plates are connected to the amplifier outputs either directly or through sampling switches.

5.6.2 Switches

The NMOS switches in the modulator have been realized using multi-finger transistors; the switch fingers share the diffusion regions.

Figure 5.16 shows the layout for the DAC-switch cluster. The switch cluster is drawn in a row parallel to the feedback-capacitor array so that the switch-to-capacitor routes are of equal length. The ϕ_2-gated thermometer-code output signals, which are DAC-bits, have been routed as a bus from the quantizers to the DAC-switch gates and have been matched in their lengths. The reference voltages feed in to the switch-cluster from the left, while the DAC signals feed in from the top and bottom, and the sampled outputs leave at the right of the cluster.

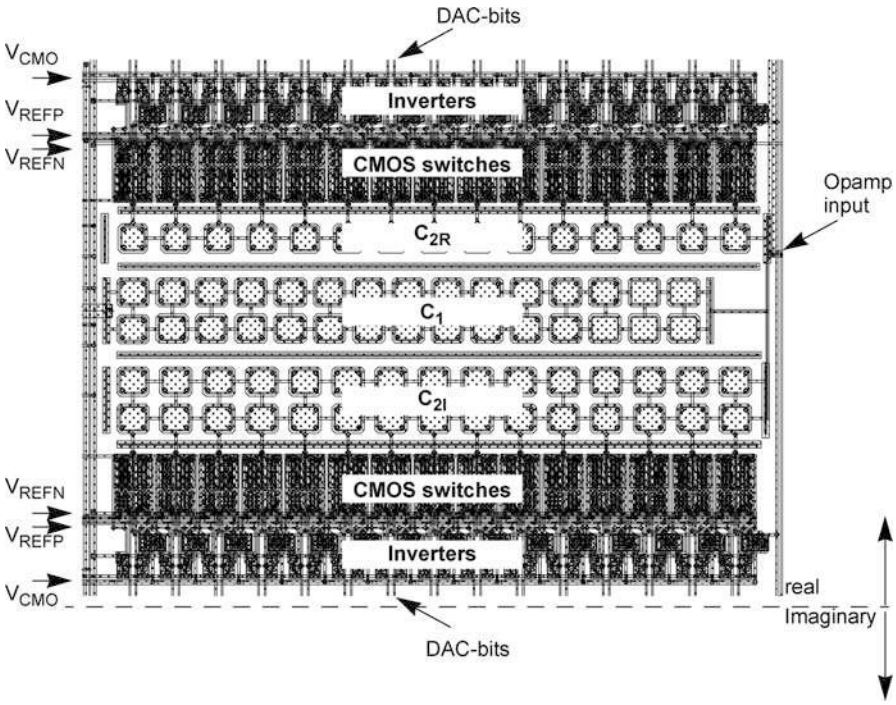


Fig. 5.16 DAC-switches and the input and feedback capacitor arrays

5.6.3 Comparators

The quantizer has been drawn in a 15×1 array, which matches the pitch of the last stage integrator. The layout in Fig. 5.17 shows a slice of the quantizer that depicts the placement and interconnections of the pre-amplifier, the regenerative latch, the R-S latch, the sampling switches, and the sampling capacitors. The sampling switches have been surrounded by P+ substrate guard rings. The separation of the comparator into analog and digital regions is evident in the layout.

5.6.4 Amplifiers

Layout strategies that employ common-centroid, dummies, identical orientations, and mirror-symmetrical arrangements [9] have been used in the layout for mismatch-sensitive analog circuits, for example, opamp, quantizer, etc. The PMOS differential pair has been drawn in a common-centroid layout. Matched devices, for example, PMOS current sources, NMOS current sinks, etc., have been drawn with interdigitated fingers that have similar orientations. For some of the devices, dummy structures have been added to ensure that mismatches due to etching are reduced.

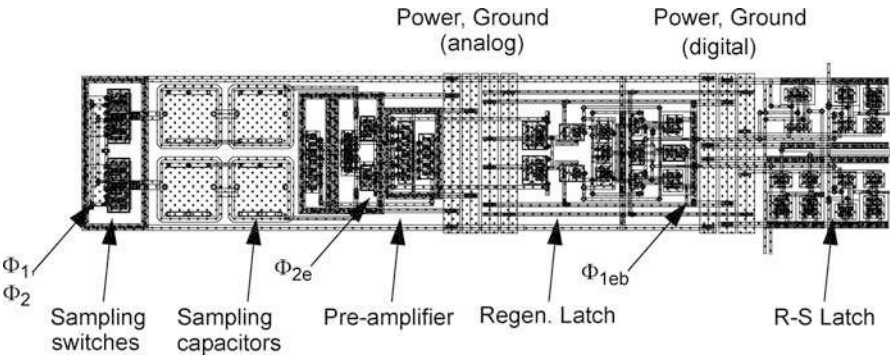


Fig. 5.17 Comparator layout

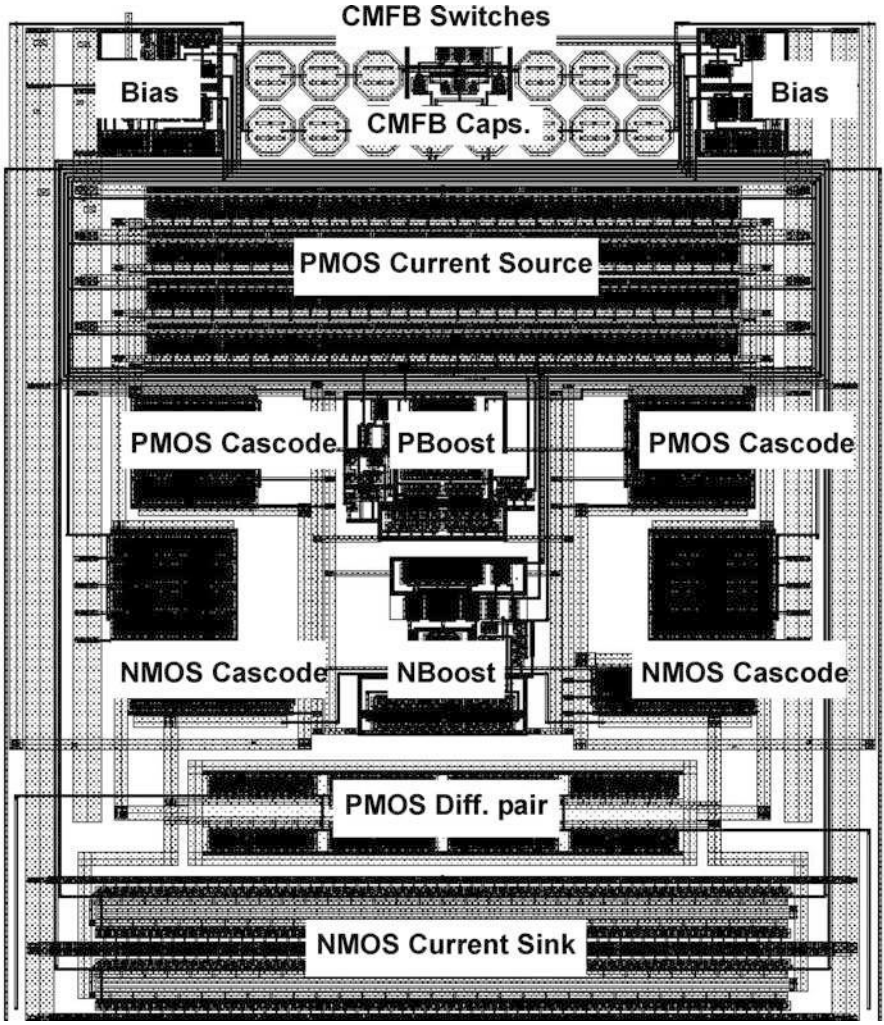


Fig. 5.18 Amplifier layout

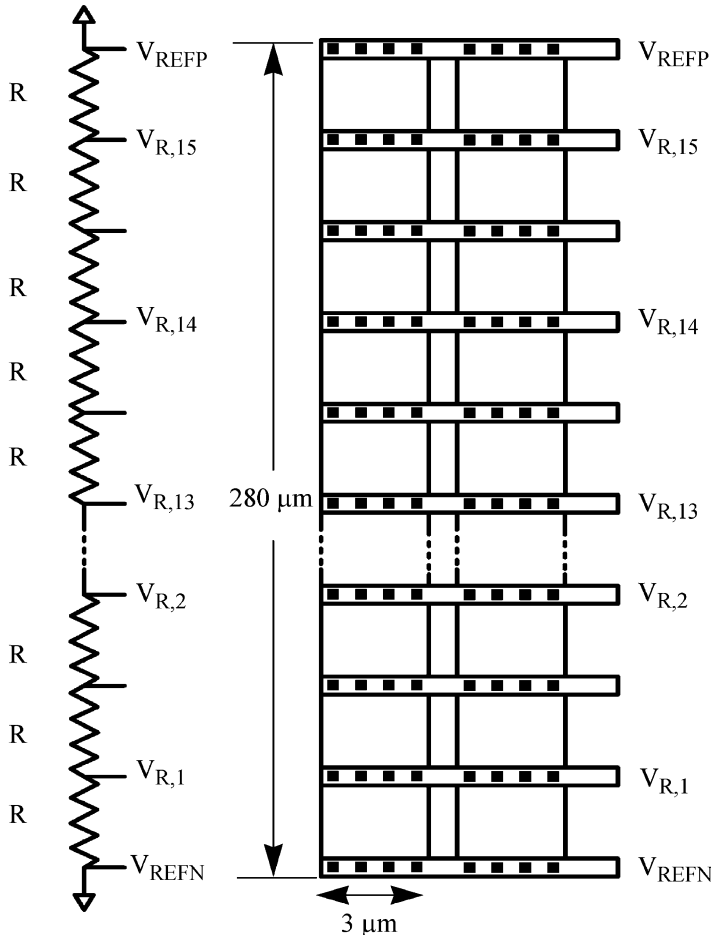


Fig. 5.19 Resistor ladder for the quantizers

The opamp biasing circuit has been divided into two unit parallel circuits in order to meet the layout symmetry. The opamp, including the bias circuits, has a horizontal symmetry. The bias circuits have been placed close to the opamp (refer to Fig. 5.18).

During routing, steps were taken to ensure that there is no wiring over the active area of the devices. The layout of the modulator was followed by an extraction of the route parasitics. The routing parasitics were balanced in order to preserve the fully-differential symmetry of the circuits.

5.6.5 The Resistor Ladder

P+ silicided polysilicon has been used to realize the resistor ladder. The resistor has been implemented with two parallel polysilicon sheets without any bends;

the parallel sheets effectively double the resistor area and thus improve the matching of the unit resistor segments (refer Fig. 5.19 for the layout diagram of the resistor ladder). To minimize errors due to contact resistance, arrays of contacts have been used to connect the voltage reference taps to the resistor ladder.

5.7 Substrate and Supply Noise Decoupling

The chip has been partitioned into analog and digital regions, and separate power supplies power the analog and digital circuits. The power supplies have been connected through separate bonding pads to off-chip voltage regulators. Well and substrate contacts have been used to improve the isolation between the analog and the digital circuits. To reduce the threshold-voltage modulation of the NMOS analog devices caused by body effect, the NMOS devices have been surrounded with a p+ substrate ring, which is connected to the local analog ground.

P+ substrate ties, which are biased to ground, and N-well guard rings, which are biased at power supply, have been placed between the sensitive analog circuits, e.g., the opamps, and between the analog and digital regions to improve the isolation between the circuits.[1] Multiple substrate contacts biased to analog ground have been placed close to sensitive analog nodes and in the unused chip area. On-chip decoupling capacitors formed of PMOS devices have been placed under the power buses and other unused chip area in order to reduce the high-frequency noise on the power supplies.

Metal-layer shielding has been used to protect signal paths and to isolate sensitive analog nodes, e.g., opamp inputs, from the noisy signals. A separate pad powers the metal-layer shield from an off-chip supply. Clocks have been distributed through buses. The clock buses have been shielded by a digital power supply in order to reduce clock noise injection through bus parasitics into the substrate, and hence into the analog ground.

The selected CMOS technology offers deep N-well, an optional layer for isolating the noise from the P-substrate. To minimize noise injection of the switching digital bits into the substrate, the I/O drivers have been realized in an isolated P-substrate, which was created by surrounding deep N-well with N-well guard ring. The power and ground for the I/O drivers have been routed from separate bonding pads.

[1] Due to the low-ohmic substrate of the selected CMOS technology, guard rings are not expected to attenuate substrate coupling significantly.

5.8 The Integrated Circuit

The proposed ΔΣ modulator was fabricated in a mixed-signal CMOS 0.18 μm six-metal single-poly technology. The chip microphotograph excluding the bonding pads is shown in Fig. 5.20. The chip, including the pads and other digital programming circuits, occupies an area of 2.15 mm^2. An overlay on the microphotograph highlights the two channels, I-channel and Q-channel, and the main blocks of the ΔΣ modulator.

5.8.1 Pins

Figure 5.21 shows the pin assignment for the modulator. The chip was packaged in a 80-pin ceramic flat pack (CFP).

The differential quadrature inputs, *Ip In* (Pins 68 and 69) and *Qp Qn* (Pins 76 and 75), feed in the chip from the top pins. The DAC references, V_{REFP} (Pin 71) and V_{REFN} (Pin 73), which are shared with the quantizer, also enter the chip from the top. V_{CMO} (Pin 72) is a "common-mode sense" output, and can be decoupled

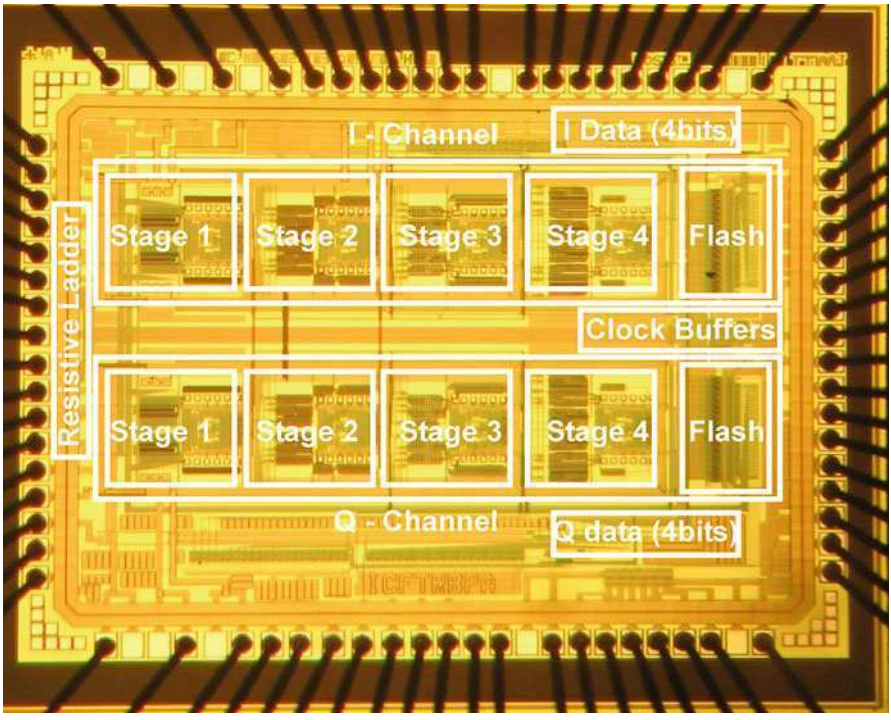


Fig. 5.20 Microphotograph of the fourth-order ΔΣ modulator

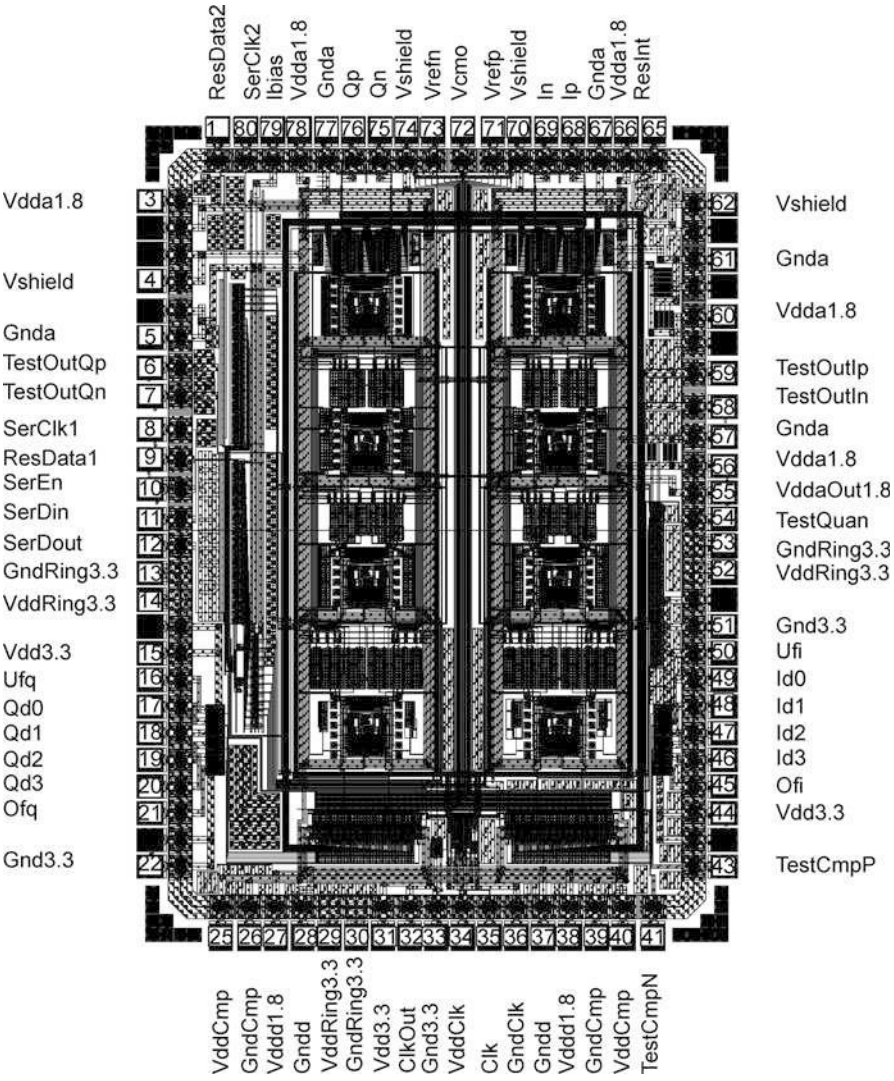


Fig. 5.21 Pin assignment for the 80-pin CFP packaging of the chip

off-chip on the PCB. *Ibias* (Pin 79) is the current-input to the master-bias current distribution block. *Vdda1.8* (Pins 3, 56, 60, 66, 78) and *Gnda* (Pins 5, 57, 61, 67, 77) provide the analog power and ground for the amplifiers and the bias circuits. *Vdd3.3* (Pins 15, 31, 42) and *Gnd3.3* (Pins 22, 33, 51) are the deep N-well power supplies for the clock-buffers and the digital-data output buffers. The chip ESD pad-ring upper and lower-voltage values have been set at 3.3 V and 0 V respectively. *VddRing3.3* (Pins 14, 29, 52) and *GndRing3.3* (Pins 13, 30, 53) are the 3.3 V power and ground supplies for the pad-ring.

Qd0-Qd3 (Pins 17–20) and *Id0-Id3* (Pins 46–49) are the 4-bit digital outputs of the modulators two channels. *Ufq*, *Ofq*, *Ufi*, and *Ofi* (Pins 16, 21, 45, 50) indicate the overflow and the undeflow status of the modulator, and, together with integrator reset pin, *ResInt* (Pin 65), can be used to reset the modulator to a known state.

5.9 The Test Set-Up

Different test set-ups were designed to characterize the performance of the prototype ΔΣ modulator. Fig. 5.22 depicts the test set-up used to measure the SNDR of the chip.

The quadrature inputs for the ADC are generated using an RF 0/90º power-splitter. A pair of 0/180° power-splitters convert the single-ended output from the 0/90° power-splitter to fully differential signals. The fully differential inputs are ac-coupled and rebiased at an input-common mode voltage of 0.7 V. The 33 Ω series termination resistors, together with the 0.47 nF value capacitor between the differential inputs, form a first-order RC anti-alias filter (refer to Fig. 5.23).

The image-rejection of the test chip was measured with quadrature input from the evaluation board CMOS DDS AD9852 [10]. To improve the image rejection of the test set-up, the output from the evaluation board was filtered with a three-stage RC polyphase filter. The three-stage RC polyphase filter shown in Fig. 5.24(a) has

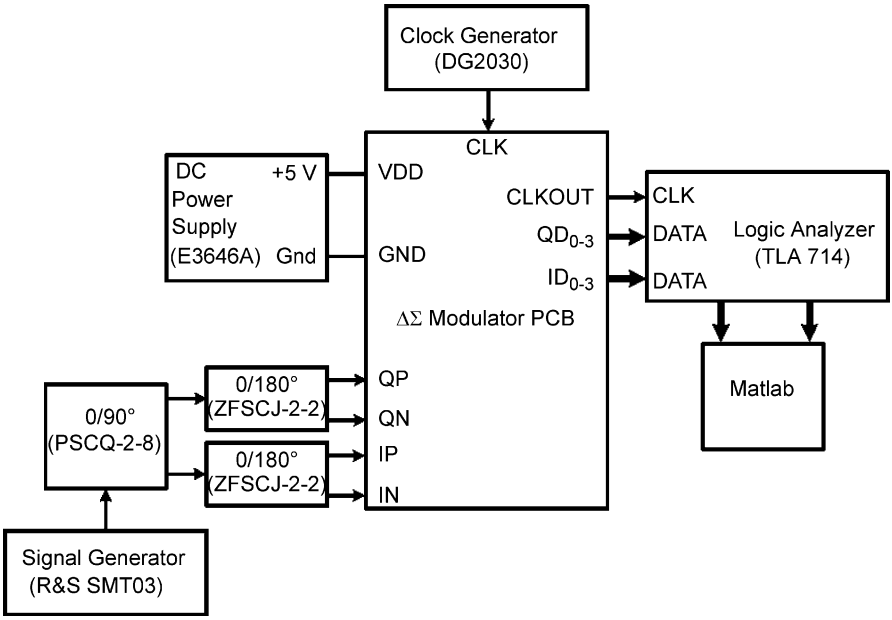


Fig. 5.22 The test set-up for measuring the SNDR of the chip

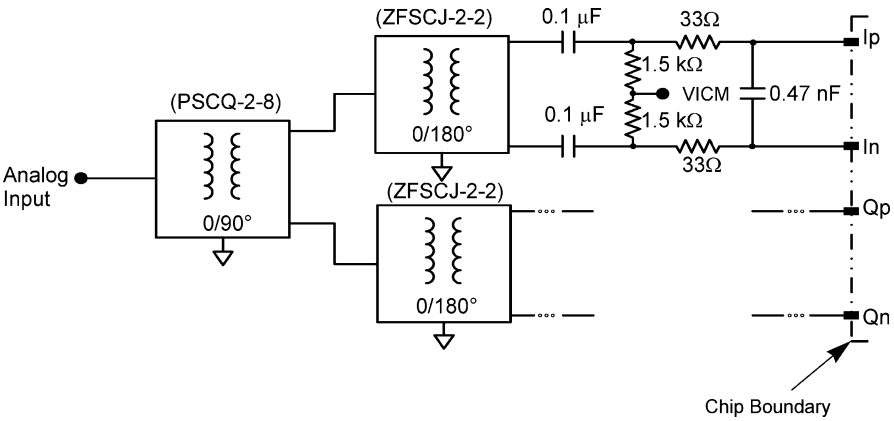


Fig. 5.23 Power-splitter-based ADC front-end

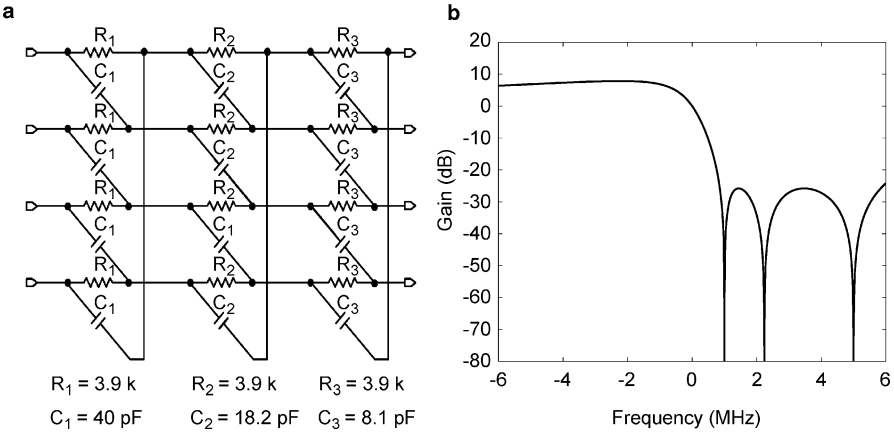


Fig. 5.24 RC Polyphase filter designed to attenuate the image at the input of the test chip: (**a**) circuit diagram showing the component values, (**b**) frequency response of the three-stage polyphase filter

been designed with pole frequencies spaced equally on the logarithmic frequency range (1–6 MHz) [11].

An 8-bit bus transceiver chip, SN74AVCH8T245, buffers the ΔΣ ADC bit-stream to the logic analyzer. Series termination resistors of value 22 Ω have been inserted between the ADC output and the transceiver inputs. The logic analyzer is edge-triggered by a clock-phase, *CLKOUT*, that is, pin 32 in Fig. 5.21, which is derived on-chip. The data from the logic analyzer is then imported into Matlab, and the *I* and *Q* data-streams are combined into a complex data-stream *I* +j*Q*. After the complex data are windowed with Hann window, the data undergoes spectrum analysis with complex-FFT. For the SNDR and other measurements of the ΔΣ modulator, 32k-bin data have been used.

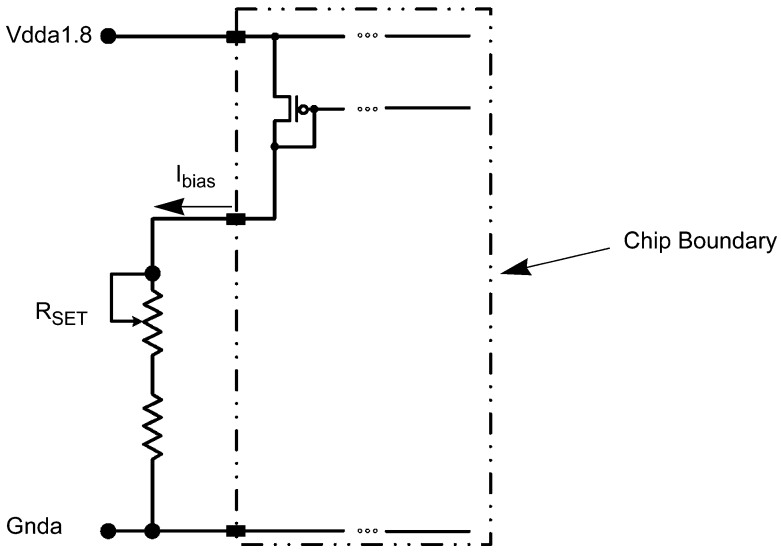


Fig. 5.25 Master bias current generation for the chip

The clock input for the ADC, *CLK*, that is, pin 35 in Fig. 5.21, is taken from a high-performance signal generator, Agilent 8664A, and rebiased using a Bias-Tee (Mini-Circuits ZFBT-4R2GW). The SN74AVCH8T245 chip buffers the clock on the PCB. During testing, the signal generator, R&S SMT03, was synchronized to an external reference generated by the clock generator, 8664A, in order to maintain a precise phase and frequency relation between the input signal and the sampling clock.

All chip voltage references have been generated using multiple voltage regulators on the PCB. The master bias current is generated using the arrangement shown in Fig. 5.25; the current I_{bias} can be varied by adjusting R_{set}.

5.10 The PCB Design

A four-layer PCB was designed for the performance characterization of the modulator (refer to Fig. 5.26). A multilayer PCB has the advantage of avoiding high-density interconnections and also thin power and ground traces to the ICs. The four layers of the PCB have been used as in [12]:

- Top-layer: The layer has been used for component mounting and signal interconnections.
- Power plane: The power plane has been split into multiple planes associated with the analog, digital, and clock-generator supplies.
- Ground plane: One layer of the PCB has been dedicated to the ground plane.
- Bottom-layer: The layer has been used for some of the non-critical component mounting and some interconnections.

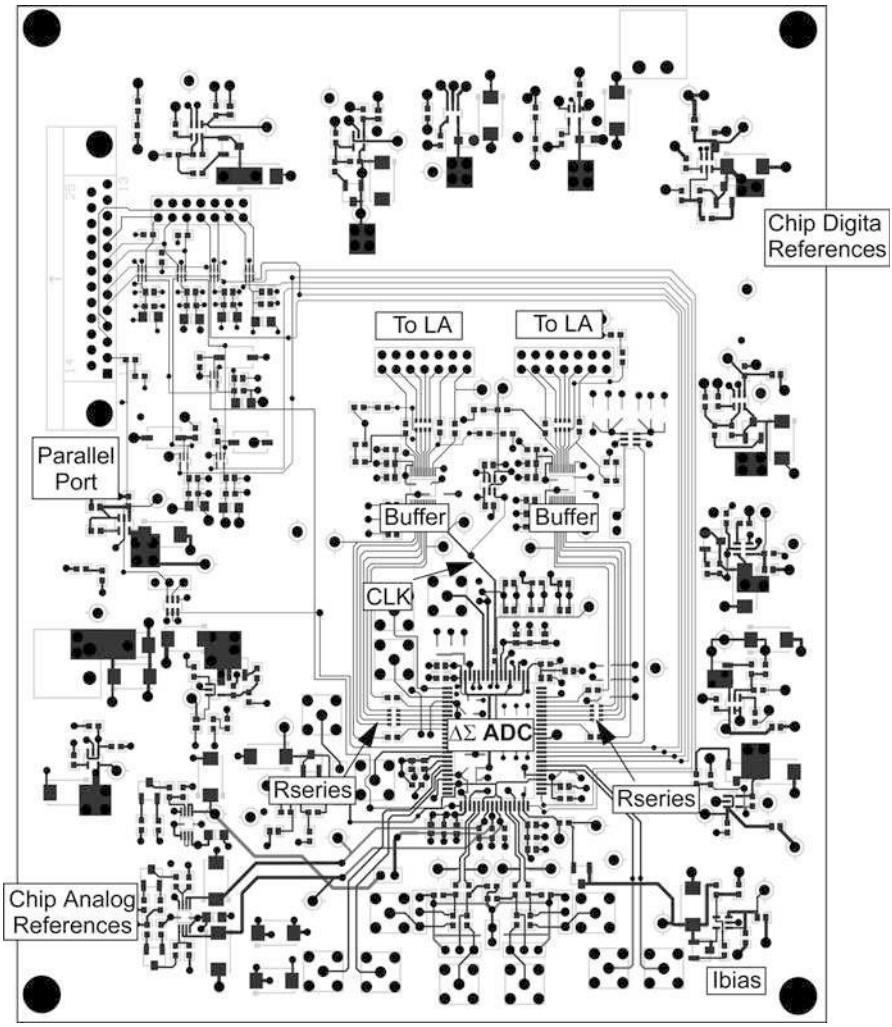


Fig. 5.26 Component side of the four-layer PCB, which was designed for testing of the ΔΣ modulator chip

Two PCBs were designed for the testing of the chip. In the first PCB design, the ground plane was split into two sub-planes separating the analog ground from the digital ground and the two planes were finally joined at the power supply. In the second PCB design, the undivided ground plane was shared between the analog and the digital grounds. Compared to the first PCB, the second PCB was less noisy, and this fact was confirmed by the SNDR measurements of the chip. The second PCB showed an improvement of 3 dB in SNDR, as compared to the first PCB. A possible reason for the degraded performance of the first PCB could be that the digital ground impedance for the split ground plane was on the higher side, and this higher

impedance was causing a crossover of the digital noise to the analog ground. In the second PCB, instead of splitting the ground plane, an effort was made to partition the routes into analog and digital sections. The component placement and layout was done in such a way to prevent cross-over of routes from one section to the other section.

Supply decoupling for the chip is achieved through a hierarchical placement of on-chip and on-PCB capacitors. The off-chip decoupling is performed using two types of surface-mounted capacitors: a bank of large electrolytic capacitors of value 100 nF and a bank of smaller ceramic capacitors of value 10 nF [13]. The ceramic capacitors are placed closer to the power pins in order to minimize the impact of parasitic lead-inductance. The decoupling capacitors, local as well as global, are connected to the ground and the power plane through interconnects of minimal lengths and, hence, of minimal parasitic inductances. Signal crossing, wherever it could not be avoided, is provided with a nearby decoupling capacitor between the power and the ground plane [14].

The chip is directly soldered to the PCB. The differential inputs to the ADC are matched in length and placed close together. Special precautions are taken to keep the digital signal traces, especially the clock signal, as far away as possible from the analog inputs and supply pins. The clock signal is routed on the top-layer, and care is taken to avoid crossing clock routes to the bottom-layer of the PCB.

5.11 Test Results

The test results of the proposed $\Delta\Sigma$ modulator are very close to the simulated results, except for a somewhat reduced maximum sampling frequency. Due to some SNR degradation issues between 105 MHz and the maximum sampling frequency of 128 MHz, the ADC testing was limited to a sampling frequency of 96 MHz. The IC achieved 70.9 dB SNDR over a 6 MHz band centered around 3 MHz. At 105 MHz, the IC performs with a loss of 3 dB in the SNDR.

Figure 5.27 shows the STF plot of the proposed $\Delta\Sigma$ ADC, which is measured at a sampling frequency of 96 MHz. The asymmetric shape of the STF plot is evident from this figure. The notch at dc in the STF plot has been caused by ac-coupling.

Figure 5.28 shows the output PSD of the chip measured for zero-input. The output spectrum reveals the complex noise shaping of the modulator and the deep notch that has been placed at the image frequency. A plot of the measured SNDR versus input amplitude is shown in Fig. 5.29. The modulator shows a dynamic range of about 75 dB for an input bandwidth of 6 MHz and a sampling frequency of 96 MHz. The modulator shows a maximum SNDR of about 71 dB for a 6 MHz input frequency at an amplitude of -3 dBFS (refer to Fig. 5.30).

Using a CMOS DDS evaluation board, AD9852, as a quadrature signal source, the image rejection of the IC was measured at a several frequencies within the 6 MHz signal bandwidth (refer to Fig. 5.31 for the test set-up used to measure the IMR of the IC). A three-stage polyphase filter was used at the IC front-end to

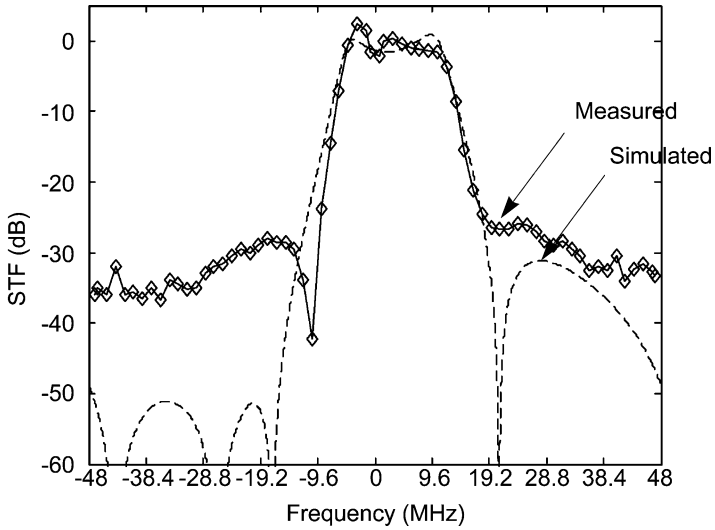


Fig. 5.27 STF measured at a sampling frequency of 96 MHz

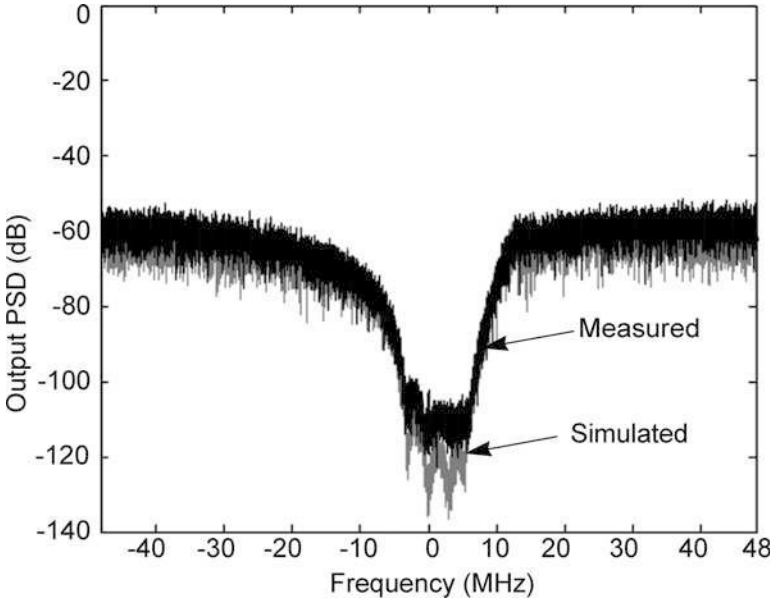


Fig. 5.28 Output PSD measured with zero-input at a sampling frequency of 96 MHz

suppress the phase and gain imbalances due to the DDS (refer to Fig. 5.24 for the details of the polyphase filter). Due to the narrow band limitation of the polyphase filter, the frequency of the input signal for the image rejection measurement was restricted to a range between 2.75 MHz and 4.5 MHz. Figure 5.32 shows the output

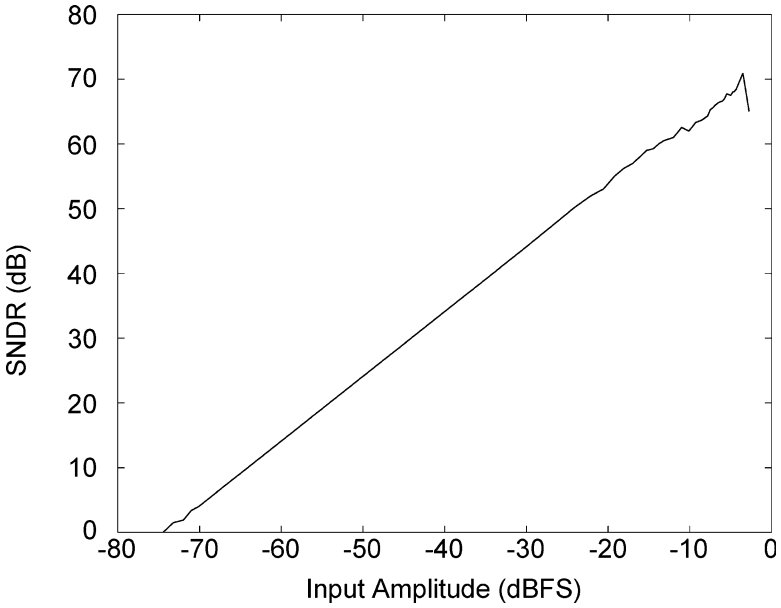


Fig. 5.29 SNDR vs. input amplitude

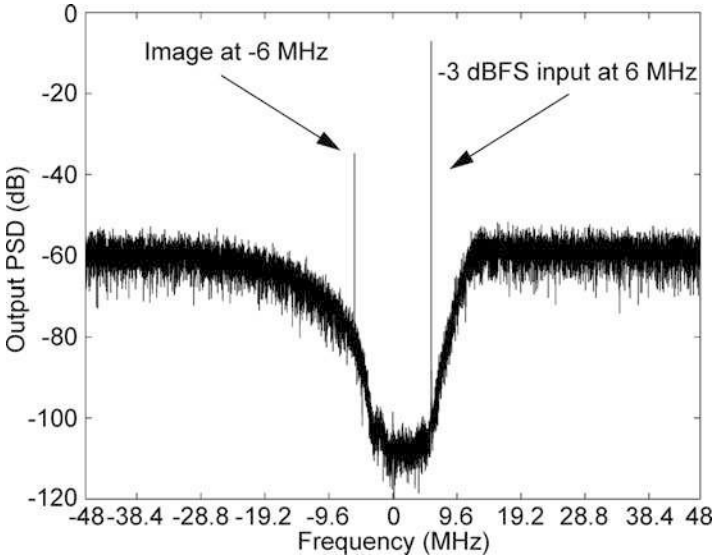


Fig. 5.30 Output PSD measured with −3 dbFS input at a sampling frequency of 96 MHz

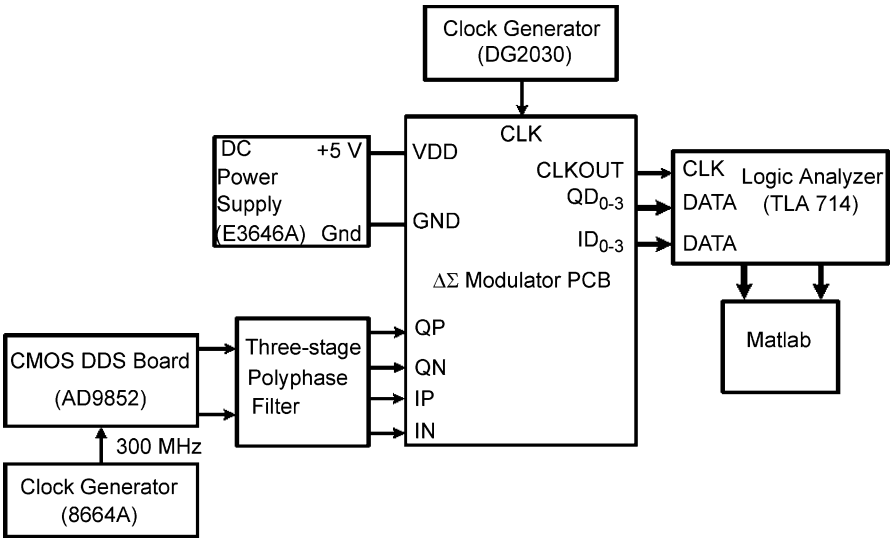


Fig. 5.31 Test set-up for measuring the IMR of the chip

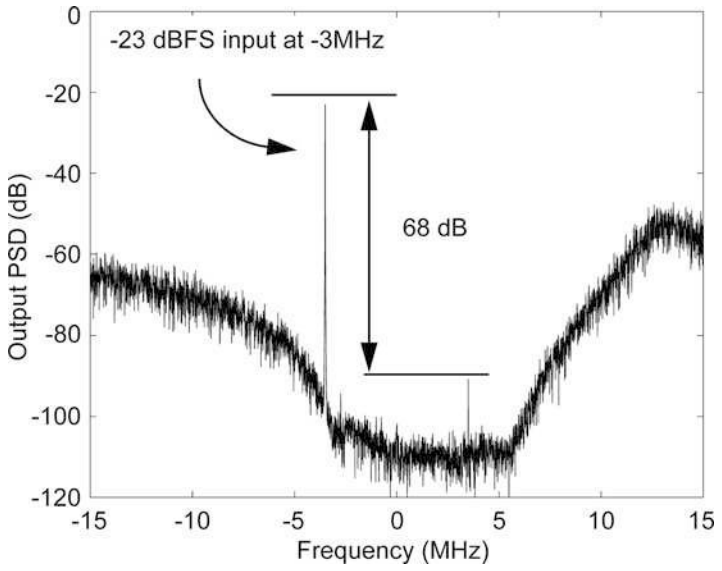


Fig. 5.32 Image rejection measurement with a three-stage polyphase filter at the input of the IC

spectrum of the ΔΣ modulator for a –3 MHz input signal. For the input signal frequencies between 2.75 MHz and 4.5 MHz, the image rejection of the ΔΣ ADC was measured as greater than 65 dB.

Figure 5.33 shows the in-band spectrum for a two-tone input (–6 dBFS each input): the IM3 product is at –69.8 dB, and the IM2 product is at –70.5 dB.

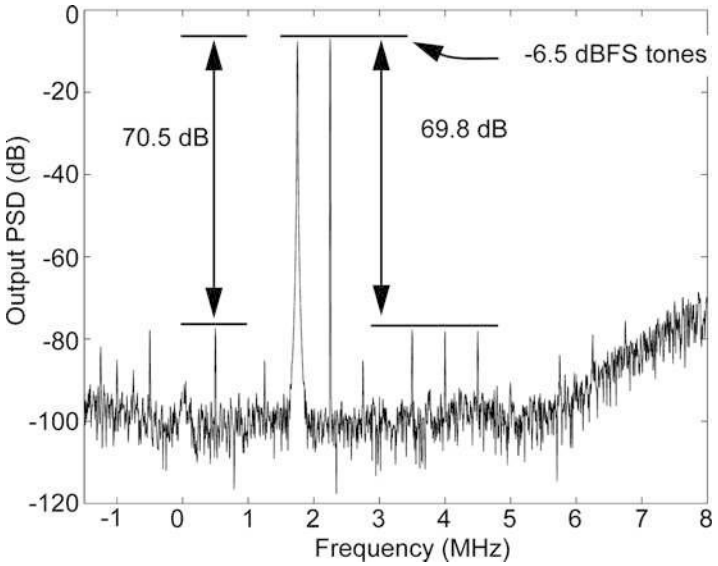


Fig. 5.33 Output spectrum of the chip for a full-scale two-tone test

Table 5.8 Summary of the simulated and measured performance of the prototype chip

	Simulated	Measured
Maximum signal bandwidth	8 MHz	7 MHz
SNDR[a]	76.4 dB	71 dB
Dynamic range	78.5 dB	75 dB
STF characteristics	>50 dB (-ve frequency)	30 dB (-ve frequency)
IMR	>65 dB	>65 dB

[a] Measured at a Sampling frequency of 96 MHz

The clock-generator consumes 29.7 mW, and the remaining ADC, including the external references, consumes 138.4 mW. The external references dissipate 9 mW.

Table 5.8 compares the simulated and the measured performance of the prototype chip.

The main differences between the measured and the simulated results have been explained in Sect. 5.13.

5.12 Performance Summary

The performance of the chip has been summarized in Table 5.9.

Table 5.10 compares the performance of the implemented ΔΣ modulator and some of the recently published complex ΔΣ modulators:

Table 5.9 Measured performance of the IC

Supply voltage	1.8 V (analog) 3.3 V (Clock)	Signal bandwidth	7 MHz
Sampling frequency	105 MHz	Diff. input range	1.6 V_{pp}
OSR	16	SNDR[a]	71 dB
Analog power (1.8 V)	122.4 mW	Area[b]	2.15 mm^2
Digital power[c] (1.8 V)	3.6 mW	DR	75 dB
Clock generator[d] (3.3 V)	29.7 mW	IMR[e]	> 65 dB
Off-chip references (1.8 V)	9 mW	SNR[a]	71.42 dB
Technology	0.18 μm 1-poly 6-metal mixed-signal CMOS		

[a] Measured at a sampling frequency of 96 MHz. At 105 MHz the SNDR degrades to 67.8 dB
[b] Includes pads
[c] Includes power consumption of the comparator and PLA
[d] Includes power of the digital buffers
[e] Measured for frequencies between 2.75 MHz and 4.5 MHz

Table 5.10 Comparison of the performance of some of the recently reported complex ΔΣ modulators

Modulator type	Signal bandwidth	OSR	IRR (dB)	SNDR (dB)	Area (mm^2)	Power (mW)
CT [15]	20 MHz	17	58	69	0.5	56 (1.2 V)
CT [16]	10 MHz	40	> 50	52	–	7 (1.2 V)
CT [17]	8.5 MHz	31	50	76	2.5	375 (3.3 V)
CT [18]	200 kHz	209	–	90	6.0	210 (1.8 V)
DT [19][a]	4 MHz	12.5	–	70.1	–	35 (1.8 V)
CT [20]	20 MHz	16	47.2	53.9	1.30	32 (2.5 V)
DT [21]	200 kHZ	32	> 75	57	0.56	18.6
CT [22]	–		> 65			4.7
CT [23]	23.0 MHz	12	> 66	68.8	0.95	42.6 (1.8 V)
DT present work	7 MHz	16	> 65	71	2.15	164.7

[a] The solution uses two low-pass ΔΣ modulators for digitizing DTV signals

Table 5.11 Comparison of the filtering characteristics of some of the recently published modulators

Modulator type	Signal bandwidth	OSR	SNDR (dB)	STF filtering characteristics
CT [24]	1 MHz	32	57	Low-pass filter, first order, $f_{3dB} = 3$ MHz
DT Present work	6 MHz	16	71	Complex filter, Stop-band attenuation >30 dB

There are not many publications regarding the design of ΔΣ modulators with a filtering STF, and, except for [31], most of the design ideas and results presented are either in the form of patents [24–26] or papers with simulation results only [27–30].

Table 5.11 shows a comparison of the STF filtering characteristics of the implemented modulator with these in [31].

5.13 Explaining the Differences Between the Measured and the Simulated Results

5.13.1 Instability and SNDR Degradation with Higher Frequencies

Two test chips mounted on two separate PCBs were tested and characterized for performance. The tests indicate that the modulators performed functionally till 105 MHz; however, beyond 105 MHz, the modulators became unstable. A PSD plot of the modulator at a sampling frequency of 100 MHz is shown in the Fig. 5.34. The magnitude plot shows a peaking at a frequency of around 15 MHz, and it was found that the peaking worsens for higher sampling frequencies. The modulator finally becomes unstable beyond the sampling frequency of 105 MHz.

A possible reason for the PSD peaking can be understood by looking at the pole-zero plot of the modulator NTF (refer to Fig. 5.35 for the pole-zero plot of the ΔΣ modulator NTF). Two relatively high Q NTF poles at $NTFP_1 = 0.84e^{j(0.25\pi)}$ and $NTFP_2 = 0.85e^{j(0.07\pi)}$ can be identified in the figure. Fortunately, the NTF pole at $0.85e^{j(0.07\pi)}$ is partially cancelled by the NTF zero at the image frequency, and it seems that the movement of the second pole towards the unit circle results in the out-of-band peaking.

Table 5.12 lists the sensitivities of the NTF poles NTF_1 and $NTFP_2$ with respect to the coefficient variations, derived with the aid of Mathematica [8].

Compared with the pole $NTFP_2$, $NTFP_1$ shows a higher sensitivity, and particularly to the variation in the coefficient B_2. To determine the SNDR degradation of the

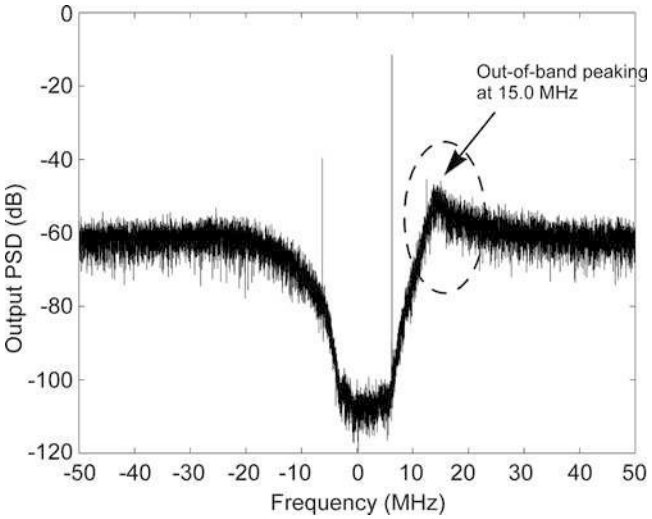


Fig. 5.34 Output PSD measured with −3 dbFS input at a sampling frequency of 100 MHz

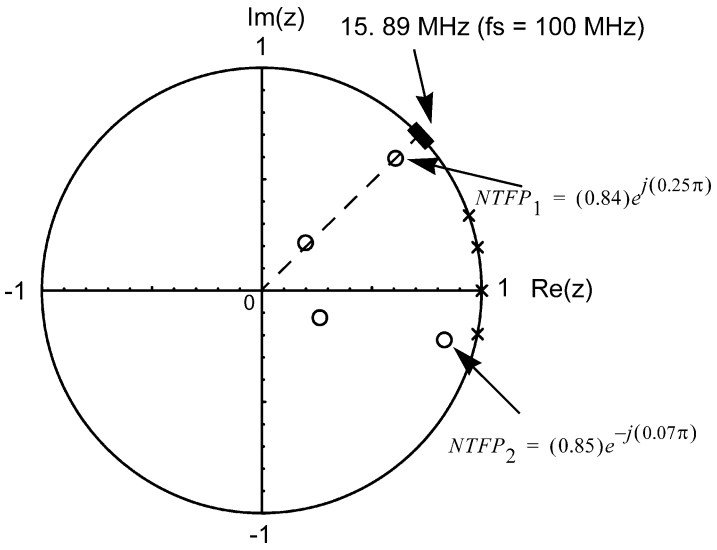


Fig. 5.35 Pole-zero plot of the ΔΣ modulator NTF

Table 5.12 Sensitivities of the NTF poles to the coefficient variations

	Sensitivity $\left(S_{C_i}^{NTFP_i} = \frac{C_i}{NTFP_i}\frac{\partial(NTFP_i)}{\partial(C_i)}\right)$	
Coefficient	$S_{C_i}^{NTFP_1}$	$S_{C_i}^{NTFP_2}$
B_1	$-0.13 + j0.4$	$-0.54 + j0.15$
B_2	$-1.0 - j1.22$	$0.33 + j0.78$
B_3	$-0.13 + j0.4$	$-0.05 - j0.46$
C_2	$-0.09 - j0.43$	$-0.13 + j0.4$
$NTFZ_1$	$-0.43 + j0.45$	$-0.04 + j0.10$
$NTFZ_2$	$0.33 + j0.72$	$0 - j0.59$
$NTFZ_3$	$-0.58 + j0.57$	$-0.02 + j0.12$
$NTFZ_4$	$-0.33 + j0.38$	$-0.18 + j0.12.$

modulator that occurs due to variation in the coefficient B_2, Monte Carlo simulations were run with no nonidealities except for a differential error of $\pm 2.5\%$ added to the B_2 coefficient (refer to Fig. 5.36a). A striking correlation that was observed was that the positive peaks of the B_2 coefficient correspond to a well-behaved output PSD plot (refer to Fig. 5.36b), whereas the negative peaks of the coefficient correspond to PSD plots with out-of-band peaking (refer to Fig. 5.36c). This behavior, taken together with the fact that the pole $NTFP_1$ has a negative sensitivity with respect to the B_2 coefficient indicates that the out-of-band peaking is related with the movement of $NTFP_1$ towards the unit circle. The coefficient variation could be due to slewing or incomplete settling of the modulator at frequencies higher than 105 MHz.

A possible reason for settling time issues could be that the wiring capacitances extracted by the extractor were underestimated. The layout parasitic extraction tool

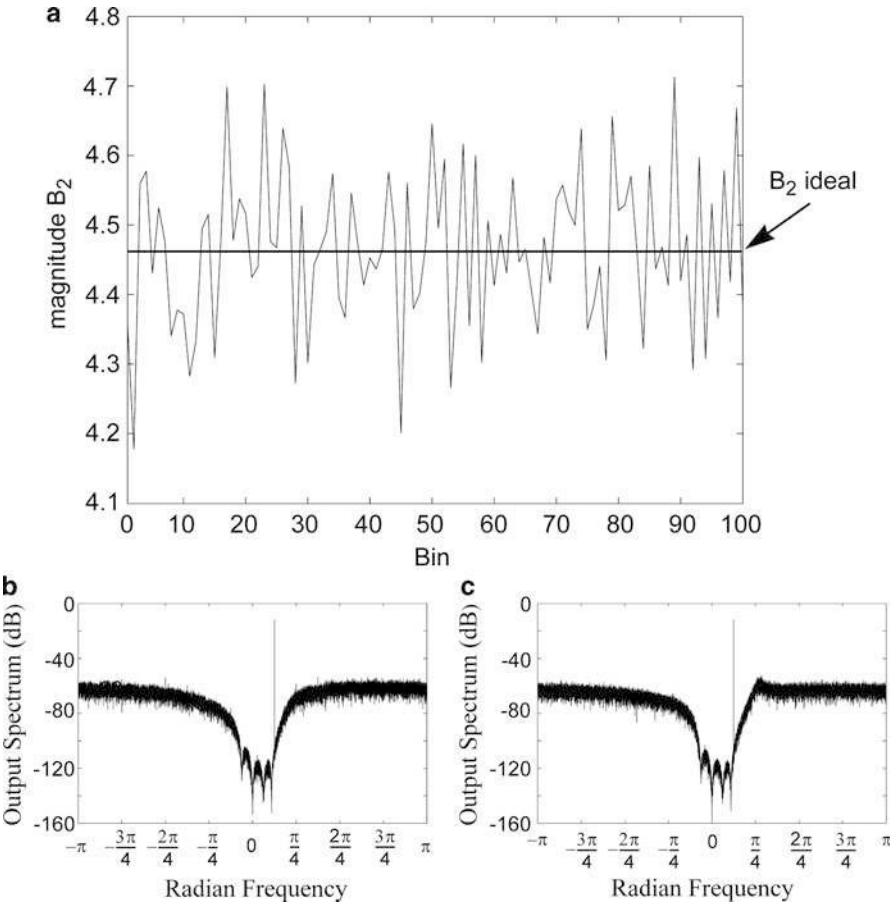


Fig. 5.36 Monte Carlo simulation with a random variation of ± 2.5% in the B2 coefficient: (**a**) variation in the B2 coefficient. Output spectrum of the ΔΣ modulator for: (**b**) bin 89, (**c**) bin 45 of the B2 coefficient

used during the layout of the chip was compared with another tool Raphael [32]. By considering a case of two metal paths on two different layers, it was found out that parasitic capacitance between two non-overlapping structures has been ignored in the parasitic extractor rule set. For example, for a nonoverlapping pair of metal paths on Metal2 and Metal3, the tool extracts the parasitic capacitance between the metals and the substrate, but fails to report any parasitic capacitance between the two metals. The suspicion that the underestimated extracted parasitic capacitances are the cause of the modulator SNR degradation and instability at a higher sampling frequency seems to be confirmed by two more observations:

- Increasing the load capacitance at the output of the second-stage integrator lowers the sampling frequency values at which the peaking and instability occur.

- Increasing the bias current to the second-stage opamp lowers the out-of-band peaking and pushes the sampling frequency at which the modulator becomes unstable to a higher value. However, after a certain point, increasing the bias currents introduces harmonic distortion in the modulator output, raises the inband noise floor, and degrades the modulator SNDR.

5.13.2 *Difference Between the Measured and the Desired STF*

Figure 5.38 shows that the measured and the desired STF agree well over the frequency band from –9.0 MHz to 19.0 MHz. However, beyond this frequency range the measured STF shows reduced attenuation compared to the STF that was targeted for this design. The behavior of the STF from –9.0 MHz to 19.0 MHz is controlled by the STF poles, and attenuation characteristics beyond this frequency range are controlled by the STF zeros. The STF zeros of the modulator have been realized by the feed-in coefficients F_1, F_2, F_3, and F_4 in the $\Delta\Sigma$ modulator architecture shown in Fig. 3.2 of Chap. 3. To determine the sensitivity of the

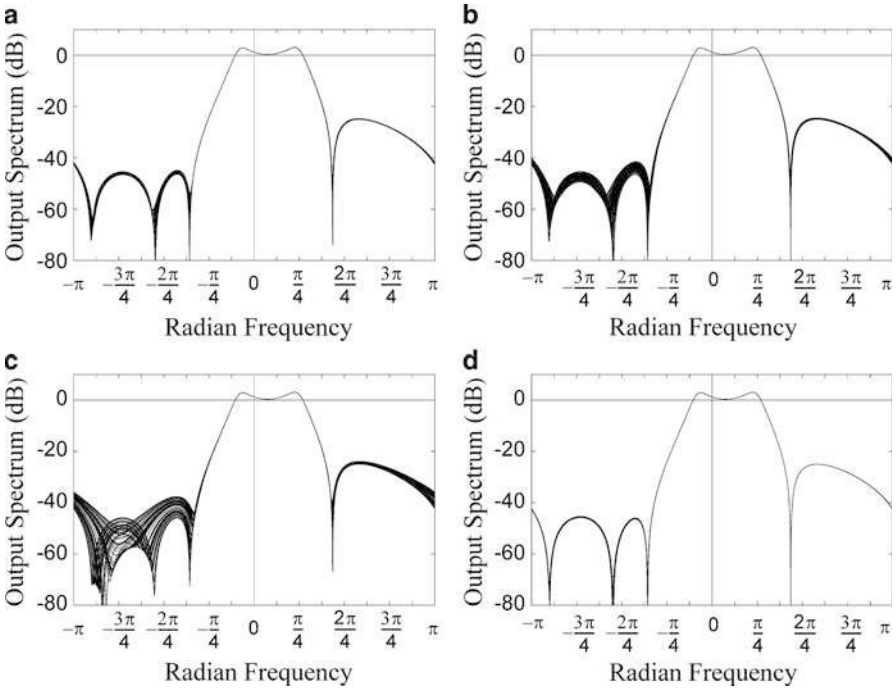


Fig. 5.37 Monte Carlo simulation with a random variation of ± 0.5% in the feed-in coefficients. STF magnitude with variation in the: (**a**) F1 coefficient, (**b**) F2 coefficient, (**c**) F3 coefficient, (**d**) F4 coefficient

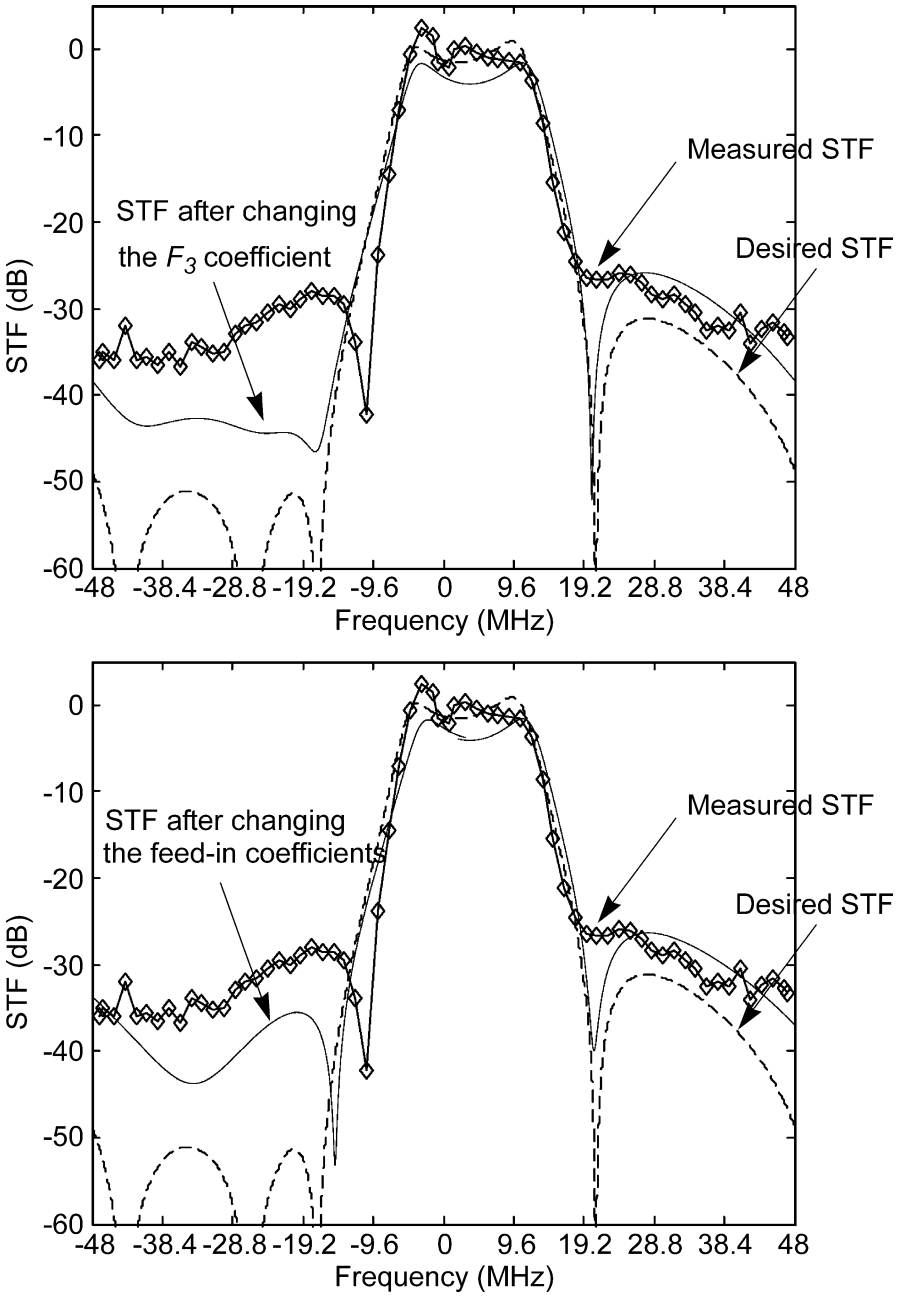


Fig. 5.38 Difference in the STF magnitude due to approximation to F_3 coefficient

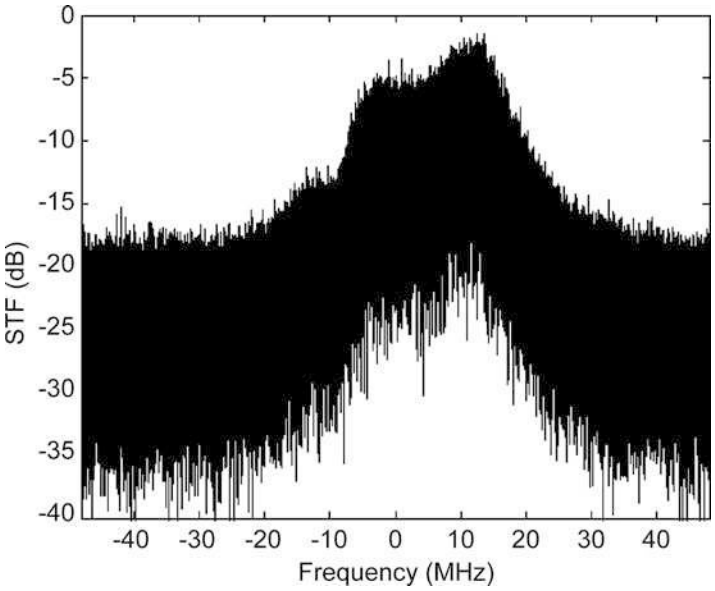


Fig. 5.39 STF magnitude plotted from the SIMULINK model

modulator STF that occurs due to variation in the coefficient F_1, F_2, F_3, and F_4 Monte Carlo simulations were run with no nonidealities except for a differential error of $\pm 0.5\%$ added to the feed-in coefficients. The STF magnitude shows a strong sensitivity to the F_3 coefficient (refer to Fig. 5.37). While inspecting the SC implementation of the modulator for the possible causes of the STF variation, it was found out that by an oversight while realizing the transfer-function zeros and poles with capacitor ratios the feed-in coefficients had been rounded to make them multiples of the feedback capacitor unit-sizes. For example, instead of realizing the coefficient $F_3 = -0.32 - 0.67I$, the rounded-down capacitor sizes realized a coefficient of value $F_3 = -0.30 - 0.67I$.

Figure 5.38a shows the impact of the rounded-down value for coefficient F_3 on the STF magnitude. Considering the sensitivity of the STF magnitude to the feed-in coefficient F_3, it would have been desirable to provide some kind of trimming for the capacitor realizing the F_3 coefficient. Figure 5.38b shows the STF magnitude for the feed-in coefficients realized in the SC implementation of the modulator. Figure 5.39 shows the STF magnitude plot derived from the SIMULINK model. The SIMULINK model includes opamp non-idealities and opamp and switch noise sources.

The modulator was simulated for any impact of coefficient approximation on the SNDR performance, however, the impact of this approximation on the STF characteristics was missed.

5.14 Power Dissipation

As can be seen from Table 5.10 the power dissipation of the proposed ADC is higher than the other recently published complex ΔΣ modulators. An exercise to optimize the opamp used in the modulator design has revealed that it is possible to upscale the PMOS devices used in the opamp by 1.5 and reduce the current consumed by 30%. By this exercise it should be possible to scale down the analog core power dissipation from 120 mW to 84 mW. At this level of power consumption, though still on the higher side, the proposed ADC is comparable to the complex ΔΣ modulator presented in [15]. A possible reason for higher power consumption could be the larger capacitors used to realize the coefficients of the modulator. This was done so that the matching between the two channels (*I* and *Q*) remains high. The IMR measurement results of the proposed ADC confirm superior matching of the *I* and *Q* channels.

References

1. D. G. Haigh and B. Singh, "A switching scheme for switched capacitor filters which reduces the effect of parasitic capacitances associated with switch control terminal," *Proc. IEEE Int. Symp. Circuits Syst.*, June 1983, vol. 2, pp. 586–589.
2. Mohammed Dessouky, and Andreas Kaiser, "Very low-voltage digital-audio ΔΣ modulator with 88-dB dynamic range using local switch bootstrapping," *IEEE J. Solid-State Circuits*, vol.36, no. 3, pp. 349–355, March 2001.
3. A. Baschirotto, and R. Castello, "A 1-V 1.8-MHz CMOS switched-opamp SC filter with rail-to-rail output swing," *IEEE J.Solid-State Circuits*, vol. 32, no. 12, pp. 1979–1986, December 1997.
4. Cadence Design Systems Inc., *Spectre*, Version 6.1.1, San Jose, California, 2006.
5. D. Senderowicz, S. F. Dreyer, J. H. Huggins, and C. A. Laber, "A family of differential NMOS analog circuits for a PCM codec filter chip," *IEEE J.Solid-State Circuits*, vol. 17, no. 6, pp. 1014–1023, December 1982.
6. Akira Yukawa, "A CMOS 8-bit high-speed A/D converter IC," *IEEE J. Solid-State Circuits*, vol. SC-20, no. 3, pp. 775–779, June 1985.
7. M. Rebeschini, and P.F. Ferguson, "Analog circuit design for ΔΣ DACs," in *Delta- Sigma Data Converters: Theory, Design, and Simulation*, S. R. Norsworthy, R. Schreier, and G. C. Temes, Eds. New York: IEEE Press, 1997, ch. 12.
8. Wolfram Research, Inc., *Mathematica*, Version 6.0, Champaign, IL., Wolfram Research, 2007.
9. A. Hastings, *The Art of Analog Layout (2nd Edition)*, ISBN 0131464108, Prentice Hall, New Jersey, 2005.
10. Analog Devices Inc., *AD9852: CMOS 300 MSPS Complete DDS*, 2007.
11. F. Behbahani, A. Karimi-Sanjaani, Wee-Guan Tan, A. Roithmeier, J.C. Leete, K. Hoshino, A. A. Abidi, "CMOS mixers and polyphase filters for large image rejection," *IEEE Journal of Solid-State Circuits*, Vol. 36, Issue. 8, pp. 873–887, June 2001.
12. Mark I. Montrose, *EMC and Printed Circuit Board: Design, Theory, and layout Made Simple (1st Edition)*, ISBN 078034703X, Wiley-IEEE Press, 1998.

13. L. D. Smith, R. E. Anderson, D. W. Forehand, T. J. Pelc, T. Roy, "Power distribution system design methodology and capacitor selection for modern CMOS technology," *IEEE Transactions on Advanced Packaging*, Vol. 22, Issue. 3, pp. 284–291, August 1999.
14. Ralph Morrison, *Grounding and Shielding Circuits and Interference (5th Edition)*, ISBN 0470097728, Wiley-IEEE Press, 2007.
15. L. J. Breems, R. Rutten, R. van Veldhoven, G. van der Weide, H. Termeer, "A 56mW CT quadrature cascaded ΔΣ modulator with 77dB DR in a near Zero-IF 20MHz band," *ISSCC Dig. Tech. Papers*, pp. 238–599, Feb. 2007.
16. S. Ouzounov, R. van Veldhoven, C. Bastiaansen, K. Vongehr, R. van Wegberg, G. Geelen, L. Breems, "A 1.2V 121-Mode CT ΔΣ modulator for wireless receivers in 90nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 242–600, Feb. 2007.
17. R. Schreier, N. Abaskharoun, H. Shibata, D. Paterson, S. Rose, I. Mehr, Q. Luu, "A 375-mW Quadrature Bandpass ΔΣ ADC With 8.5-MHz BW and 90-dB DR at 44 MHz," *IEEE Journal of Solid-State Circuits*, Vol. 41, Issue. 12, pp. 2632–2640, December 2006.
18. Paulo G. R. Silva, L. J. Breems, Kofi A.A Makinawa, Raf Roovers, Johan H. Huijsing, "An 118dB DR CT IF-to-baseband ΔΣ modulator for AM/FM/IBOC radio receivers," *ISSCC Dig. Tech. Papers*, pp. 66–637, Feb. 2006.
19. Yoshihisa Fujimoto, Yusuke Kanazawa, Pascal Lore, Masayuki Miyamoto, "An 80/100MS/s 76.3/70.1dB SNDR ΔΣ ADC for digital TV receivers," *ISSCC Dig. Tech. Papers*, pp. 76–639, Feb. 2006.
20. Jesus Arias,Peter Kiss, Vladimir Prodanov, Vito Boccuzzi, Mihai Banu, David Bisbal, Jacinto San Pablo, Luis Quintanilla, and Juan Barbolla, "A 32-mW 320-MHz Continuous-Time Complex Delta-SigmaADC for Multi-Mode Wireless-LAN Receivers," *IEEE Journal of Solid-State Circuits*, vol. 41, pp. 339–351, Feb 2006.
21. Kong-Pang Pun, Wang-Tung Cheng, Chiu-Sing Choy, Cheong-Fat Chun, "A 75-dB image rejection IF-input quadrature-sampling SC ΔΣ modulator," *IEEE Journal of Solid-State Circuits*, Vol. 41, Issue. 6, pp. 1353–1363, June 2006.
22. F. Munoz, K. Philips, A. Torralba, "A 4.7mW 89.5dB DR CT complex ΔΣ ADC with built-in LPF," *ISSCC Dig. Tech. Papers*, pp. 500–613, Feb. 2005.
23. Navid Yaghini, David Johns, "A 43mW CT complex ΔΣ ADC with 23MHz of signal bandwidth and 68.8dB SNDR," *ISSCC Dig. Tech. Papers*, pp. 502–613, Feb. 2005.
24. John Laurence Melanson, "Delta-sigma modulators with integral digital low-pass filtering," United States Patent, *US 7,116,721*.
25. Yann Le Guillou, "Feedforward sigma-delta AD converter with an optimized builtin filter function," European Patent, *WO 2007/066273*.
26. Yann Le Guillou, Hussein Fakhoury, "Continuous-time sigma-delta analog-todigital converter with non-invasive filters(s) for immunity preservation against interferers," European Patent, *WO 2006/054214*.
27. M. Ranjbar, O. Oliaei, "Continuous-time feed-forward ΣΔ- modulators with robust signal transfer function," *Electronics Letters*, vol. 43, no. 24, pp. 1878–1881, 22nd November 2007.
28. N. Jouida, N. C. Rebai, A. Ghazel, "Built-in Filtering for Out-of-Channel Interferers in Continuous-Time Quadrature Bandpass Delta Sigma Modulators," *ICECS*, pp. 947–950, December 2007.
29. Y. Le Guillou, H. Fakhoury, "Elliptic filtering in continuous-time sigma-delta modulato," *Electronics Letters*, vol. 41, no. 4, pp. 167–168, 17th February 2007
30. N. Beilleau, H. Abouushady, and M. M. Louerat, "Filtering adjacent channel blockers using signal-transfer-function of continuous-time ΔΣ modulators," *IEEE Midwest symposium on circuits and systems*, July 2004.
31. K. Philips, P.A.C.M. Nuijten, R.L.J. Roovers, A.H.M. van Roermund, F.M. Chavero, M.T. Pallares, A. Torralba, "A continuous-time ΣΔ ADC with increased immunity to interferers," *IEEE Journal of Solid-State Circuits*, Vol. 39, Issue. 12, pp. 2170–2178, December 2004.
32. Synopsys, Inc., *Raphael- Interconnect Analysis Tool*, Mountain View, CA, 2005.

Chapter 6
Conclusions

A digital receiver architecture based on a new low-IF *complex* ΔΣ modulator with filtering STF has been proposed in this book. A methodology for designing the filtering STF has also been proposed. A thorough examination through simulations (Matlab, Spectre, etc.,) was followed by a silicon implementation of a SC prototype modulator.

6.1 Contributions

This book presents an oversampling complex bandpass ΔΣ ADC with a signal transfer function that achieves a significant filtering of interfering signals. A filtering ADC reduces the complexity of the receiver by minimizing the requirements of analog filters in the IF digitization path. Unlike the continuous time ΔΣ modulator ADCs discussed in the literature, this discrete-time ΔΣ modulator ADC with an STF that significantly filters interfering signals is the first one of its kind reported.

The ΔΣ modulator signal transfer function (STF) and noise transfer function (NTF) have been designed using complex filter routines based on classical filter design procedures. With a filtering STF and stop band attenuation greater than 30 dB, the ΔΣ modulator reduces intermodulation of the desired signal and the interfering signals at the input of the quantizer, and also avoids feedback of the high-frequency interfering signals at the input of the modulator.

The reported complex ΔΣ ADC is intended for DTV receiver applications. With a maximum intended sampling frequency of 128 MHz and an OSR of 16, the ADC has been designed to support a maximum DTV signal bandwidth of 8 MHz. The ADC has been tested up to a maximum sampling frequency of 105 MHz. The IC achieved 70.9 dB SNDR over a 6 MHz band centered around 3 MHz. The image rejection ratio (IRR) of the ΔΣ ADC was measured as greater

B. Pandita, *Oversampling A/D Converters with Improved Signal Transfer Functions*, Analog Circuits and Signal Processing, DOI 10.1007/978-1-4614-0275-6_6,

than 65 dB. The out-of-band rejection of the ADC has been measured as greater than 30 dB. The key contributions of this book are:

- A new method for obtaining optimal NTF and STF in the design of ΔΣ modulators. The approach uses a norm based criterion and allows an STF with the desired frequency response specification. The technique has been applied to the cases of real and complex ΔΣ modulator transfer function designs.
- The severe SNDR degradation in the traditional input-feedforward ΔΣ modulators in presence of DAC non-linearities has been identified. For the input-feedforward ΔΣ modulator, the interfering tones at the output of the quantizer remain of the same magnitude as at the input. The large out-of-band quantization noise and the interfering tones are aliased back in-band due to the DAC non-linearity resulting into a severe SNDR degradation. The proposed ΔΣ modulator by filtering these out-of-band interfering signals shows an increased robustness to DAC non-linearities.
- A feedforward ΔΣ modulator architecture without the limitations of the traditional feedforward architectures has been proposed. The architecture avoids weighted summation at the quantizer input. The STF of the modulator is well controlled and robust in present of mismatches and other non-linearity. The well controlled bandpass nature of the STF makes the ADC ideal for wireless signals.
- Chapters 4 and 5 discuss the behavioral and circuit implementation of the modulator. The techniques of noise analysis and capacitor sizing have been extended from the real ΔΣ modulator case and applied to the study of complex delta-sigma modulator. Circuit techniques suitable for the realization of the modulator have been developed. The modulator avoids issues related to clock-boosting by using thick oxide devices for the switches. The feedforward coefficients have been realized by a sum of non-delaying and a differencing coefficient.

6.2 Suggestions for Future Work

6.2.1 Continuous-time Modulator Architectures

Continuous-time modulators with implicit antialias filtering seem to be better suited for digitization of channels that are accompanied by very high adjacent interferers. Compared to switched-capacitor implementation, continuous-time modulator also have lower power consumption. However, a switched-capacitor modulator is more robust to clock jitter and process variations. A continuous-time or preferably a hybrid implementation of the low-IF complex ΔΣ modulator may be a useful step.

6.2.2 Frequency-Translating Complex ΔΣ Modulator

A possible IF-to-baseband conversion architecture could incorporate a quadrature mixer inside the loop of the baseband modulator. The IF input signal is mixed with the LO frequency and translated to the baseband by the mixer in the forward path. The feedback signal is upconverted by a second mixer to match the downconverting mixer in the forward path. A main advantage of placing the mixer in the forward path is that its nonidealities are suppressed by the loopgain. The nonidealities of the mixer in the feedback path are not suppressed by the loopgain, but, by a careful selection of the LO frequency and the sampling frequency, the frequency upconversion in the feedback path can easily be performed in the digital domain with perfect linearity.

6.2.3 Demodulator Architectures

A next step would be to construct a complete system for demodulation of the digital TV signal. The high dynamic range, presence of interferers, and digital modulation may reveal further architecture requirements that are not understood yet. It would be of interest to include a channel mismatch cancellation strategy and to verify its feasibility for the low-IF complex ΔΣ modulator.

Appendix A
Modulator Design Example

This appendix introduces the various functions and design procedures written in Matlab, Simulink, and Mathematica that were used in the designing of the complex ΔΣ ADC discussed in this book.

Modulator Transfer-Function Design

The ΔΣ modulator signal transfer function (STF) and noise transfer function (NTF) have been designed using complex filter routines based on classical filter design procedures. Once the transfer functions are determined, the modulator coefficients are solved by using the symbolic equation solving capabilities of Mathematica.

B. Pandita, *Oversampling A/D Converters with Improved Signal Transfer Functions*, Analog Circuits and Signal Processing, DOI 10.1007/978-1-4614-0275-6,

Determining Coefficients with Mathematica Figures A.1–A.5

This section deals with initialization.

```
In[221]:= OSR = 16; BW = 8×10^6; f0 = 4.0×10^6;
          fs = OSR * BW; Ω = 2 π 1.0/fs;
          p1 = E^(I 0.0×10^6 Ω); (* 0.0 MHz *)
          p2 = E^(I (7×10^6 Ω)); (* 7 MHz *)
          p3 = E^(I 4×10^6 Ω); (* 4 MHz *)
          p4 = E^(-I 4×10^6 Ω); (* -4 MHz *)
          {p1, p2, p3, p4}
Out[227]= {1. + 0. i, 0.941544 + 0.33689 i, 0.980785 + 0.19509 i, 0.980785 - 0.19509 i}

In[228]:= ntfpoles = Import["ntfpoles.txt", "Table"];
          ntfp1 = ntfpoles[[1, 1]] + I ntfpoles[[1, 2]];
          ntfp2 = ntfpoles[[2, 1]] + I ntfpoles[[2, 2]];
          ntfp3 = ntfpoles[[3, 1]] + I ntfpoles[[3, 2]];
          ntfp4 = ntfpoles[[4, 1]] + I ntfpoles[[4, 2]];
          {ntfp1, ntfp2, ntfp3, ntfp4}
Out[233]= {0.830904 - 0.221809 i, 0.607757 + 0.593772 i,
           0.264252 - 0.122771 i, 0.197154 + 0.21455 i}

In[234]:= stfzeros = Import["stfzeros.txt", "Table"];
          stfz1 = stfzeros[[1, 1]] + I stfzeros[[1, 2]];
          stfz2 = stfzeros[[2, 1]] + I stfzeros[[2, 2]];
          stfz3 = stfzeros[[3, 1]] + I stfzeros[[3, 2]];
          stfz4 = stfzeros[[4, 1]] + I stfzeros[[4, 2]];
          stfk = stfzeros[[5, 1]] + I stfzeros[[5, 2]];
          {stfz1, stfz2, stfz3, stfz4, stfk}
Out[240]= {0.2024 + 0.9793 i, -0.9433 - 0.2943 i,
           0.4313 - 0.9022 i, -0.1471 - 0.9891 i, 0.03 + 0. i}
```

Fig. A.1 Mathematica code for initializing the coefficient determination for the STF and the NTF

This section deals with the NTF derivation.

```
In[241]:= L1 = (z/(z - p2)) (1/(z - p3)) (z/(z - p4)) + B1 (1/(z - p3)) (z/(z - p4)) + (B2 + B3 z^-1) (z/(z - p4)) (1/(z - p1));
          Hgen = 1/(1 + C2 L1);
          Hgen = Factor[Hgen];
          Hgen = Together[Hgen];
          Hden = Denominator[Hgen];
          t1 = CoefficientList[Hden, z];

In[247]:= NTF = ((z - p1) (z - p2) (z - p3) (z - p4))/((z - ntfp1) (z - ntfp2) (z - ntfp3) (z - ntfp4));
          Nden = Denominator[NTF];
          t2 = CoefficientList[Nden, z]

Out[249]= {0.0382915 + 0.0488114 i, -0.361626 - 0.299796 i,
           1.3448 + 0.694716 i, -1.90007 - 0.463742 i, 1}

In[250]:= sol = Solve[t1 == t2, {B1, B2, B3, C2}]

Out[250]= {{B1 → 2.51467 - 0.66127 i, B2 → 8.89598 - 10.22 i,
            B3 → -3.33592 + 5.46227 i, C2 → 0.104122 + 0.10536 i}}
```

Fig. A.2 Mathematica code for determining the coefficients of the NTF

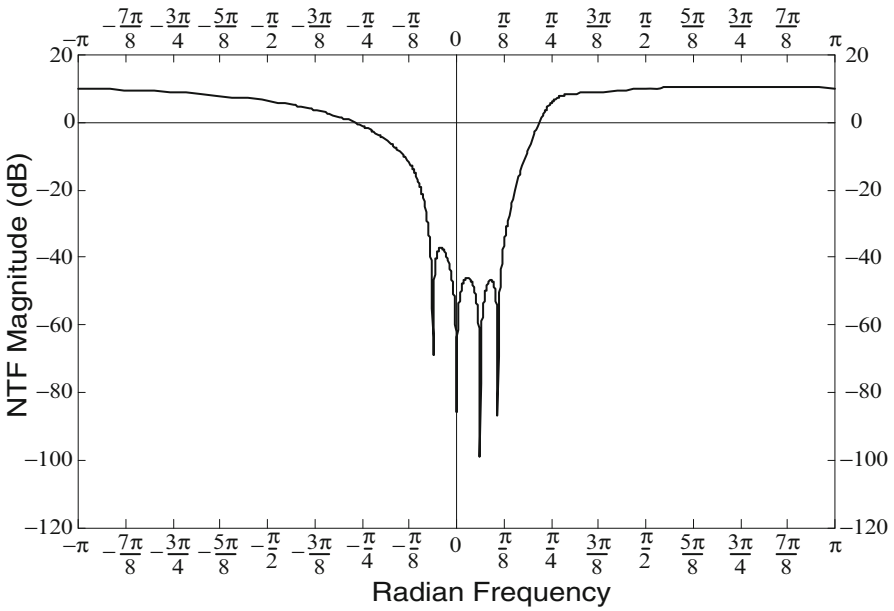


Fig. A.3 Plot of the NTF in Mathematica

This section deals with the STF derivation.

```
In[253]:= S1 = C1 L1 / (1 + C2 L1);

          S2 = (F1) z/(z-p2) 1/(z-p3) z/(z-p4) / (1 + C2 L1);

          S3 = (F2) 1/(z-p3) z/(z-p4) / (1 + C2 L1);

          S4 = (F3 z^-1 + F4) z/(z-p4) / (1 + C2 L1);

          Ggen = S1 + S2 + S3 + S4;
          Ggen = Factor[Ggen];
          Ggen = Together[Ggen];
          Gnum = Numerator[Ggen];
          STF = stfk (z - stfz1) (z - stfz2) (z - stfz3) (z - stfz4) / ((z - ntfp1) (z - ntfp2) (z - ntfp3) (z - ntfp4));
          Snum = Numerator[STF];
          s1 = CoefficientList[Gnum, z] /. sol2
          s2 = CoefficientList[Snum, z];
          sol3 = Solve[s1 == s2, {F1, F2, F3, F4, C1}];
          sol4 = sol3[[1]];
          (*{F1,F2,F3,F4,C1}={F1,F2,F3,F4,C1}/.sol2*)
          coeffs = Union[sol2, sol4];

Out[263]= {(-5.66948 + 2.97014 i) C1 - (0.857729 + 0.514103 i) F3,
           (19.6126 - 13.1427 i) C1 + (0.941544 + 0.33689 i) F2 + (2.78006 + 1.04608 i) F3 -
            (0.857729 + 0.514103 i) F4, (-22.3591 + 19.7147 i) C1 - (1. + 0. i) F1 -
            (1.94154 + 0.33689 i) F2 - (2.92233 + 0.53198 i) F3 + (2.78006 + 1.04608 i) F4,
           (8.89598 - 10.22 i) C1 + 1. F1 + 1. F2 + 1. F3 - (2.92233 + 0.53198 i) F4, 1. F4}
```

Fig. A.4 Mathematica code for determining the coefficients of the STF

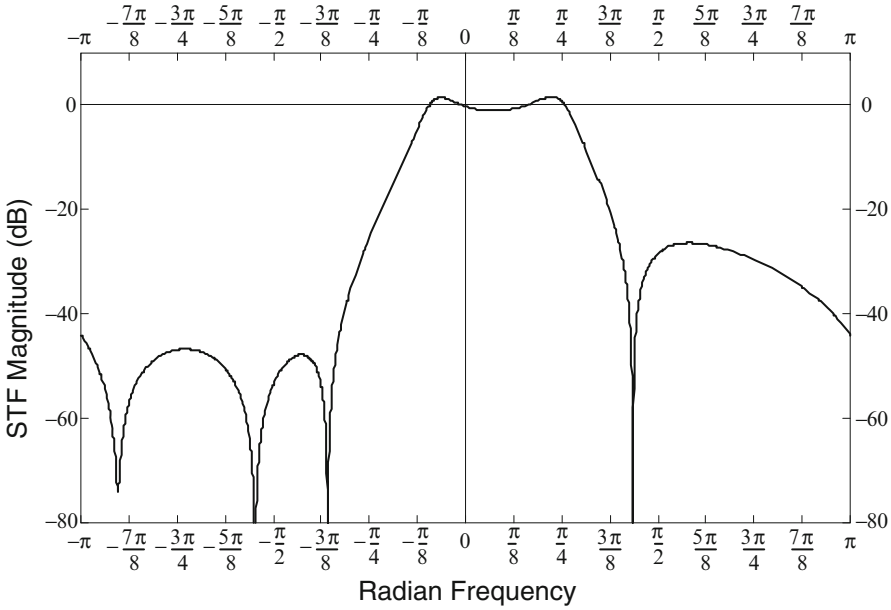


Fig. A.5 Plot of the STF in Mathematica

Simulink Model of the Complex ΔΣ Modulator

Figure A.6 presents the behavioral model of the fourth-order complex ΔΣ modulator developed in Simulink. The only difference between this modulator model and any other real ΔΣ modulator model is that the model shown uses complex coefficients. The coefficients listed in Table A.1 were used in model simulation. Simulink is used to implement the modulator architecture and model non-idealities like finite dc gain, finite bandwidth, opamp saturation, switched capacitor noise and other characteristics. The model presented in Fig. A.7 differs

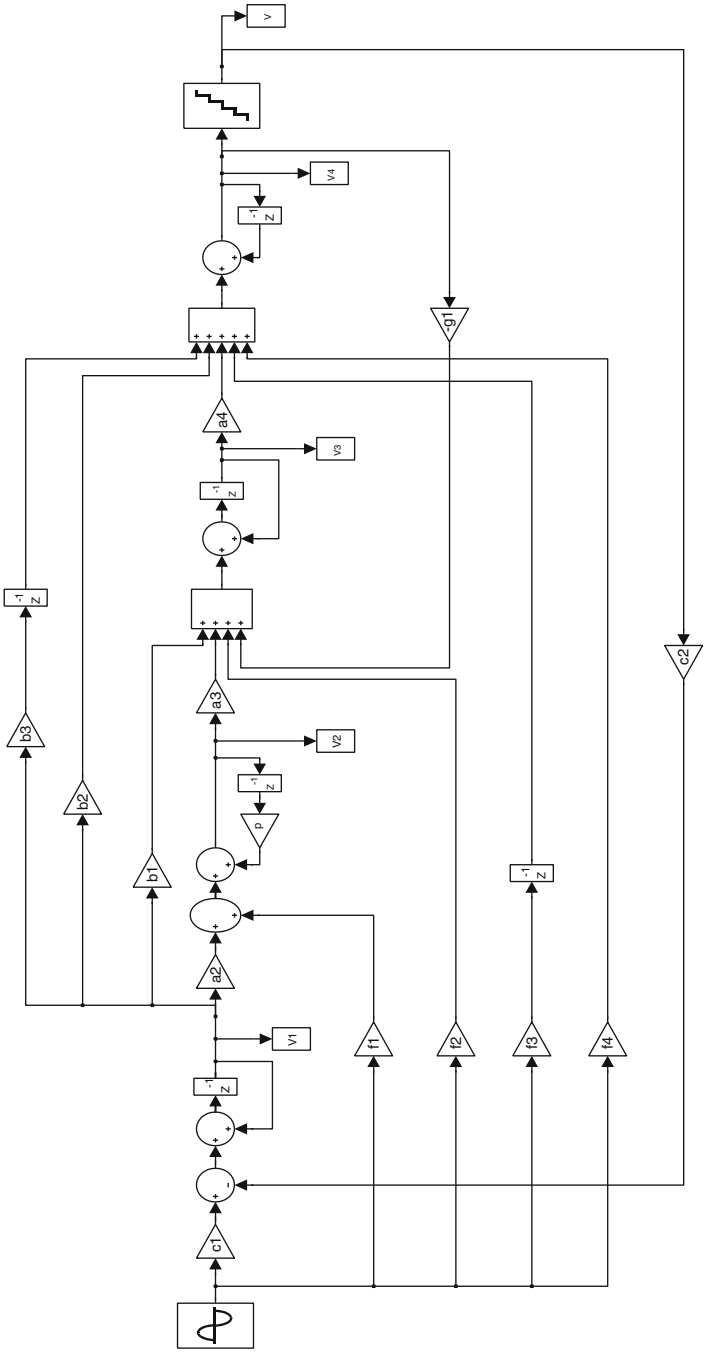


Fig. A.6 Simulink model of the complex $\Delta\Sigma$ modulator

Table A.1 Coefficient sizes

Coefficient	Value
C_1	0.3426
C_2	$0.18 - i0.41$
A_2	$-0.28 + i0.73$
A_3	0.27
A_4	1.5
$\boldsymbol{B_1}$	$0.24 + i0.49$
B_2	$2.0 + i3.93$
B_3	$-0.93 - i1.88$
F_1	$-0.24 - i0.65$
F_2	$-0.14 - i0.24$
F_3	$-0.31 - i0.67$
F_4	0.02

from the previous presented model by depicting the I and Q paths of the modulators. The model closely matches the way the modulator has been implemented in schematic. It is possible to introduce mismatches in the I and Q paths and assess the impact of mismatches on image rejection and SNDR. The code listing presented in Fig. A.8 presents a possible way to introduce mismatches and perform a Monte Carlo simulation of the Simulink model.

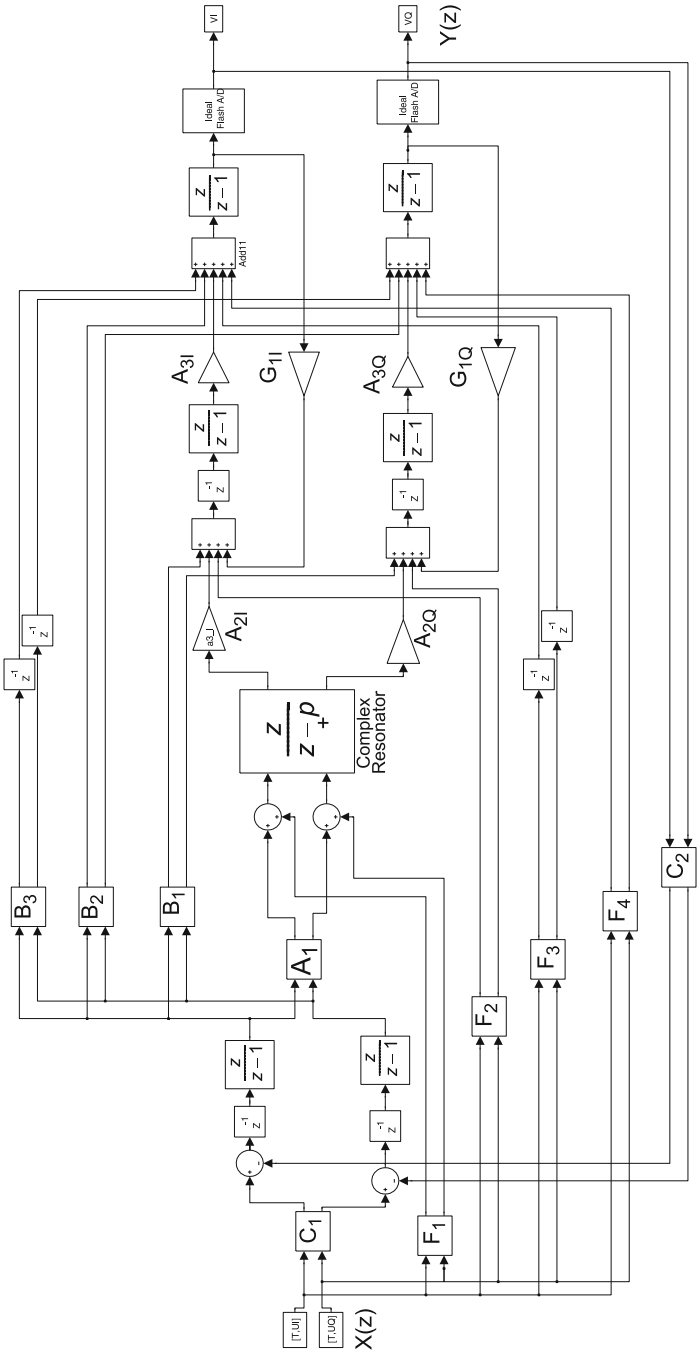


Fig. A.7 Simulink model of the complex $\Delta\Sigma$ modulator

Monte Carlo Simulation of the Simulink Model

```
%Code for MonteCarlo Simulation of the IQ Simulink Model
%Number of coefficents =13
Num_Coeffs=13;
dev=5; %Ten Percent deviation
    CAPS_I=[]; CAPS_Q=[];
    for i=1:100
        sigmai = randn(1,Num_Coeffs);
        sigmai = (dev/100 / std(sigmai)) * (sigmai - mean(sigmai));
        sigmaq = randn(1,Num_Coeffs);
        sigmaq = (dev/100 / std(sigmaq)) * (sigmai - mean(sigmaq));
        CAPS_I = [CAPS_I (1+sigmai)'];
        CAPS_Q = [CAPS_Q (1+sigmaq)'];
    end
    save CAPSI_100 CAPS_I
c1 =  0.3426;              c2 = 0.1856 - 0.4105i;
f1 = -0.2438 - 0.6574i;    f2 = -0.1440 - 0.2461i;
f3 = -0.3185 - 0.6693i;    f4 = 0.0233 + 0.0000i;
g1 =  0.0256;              a2 = -0.2830 + 0.7366i;
a3 =  0.2778;              a4 = 1.5;
b1 =  0.2428 + 0.4909i;    b2 = 2.0877 + 3.9354i;
b3 = -0.9330 - 1.8862i;
mcruns =100;              %Number of MonteCarlo runs
for i=1:mcruns
    caps_i=CAPS_I(1:Num_Coeffs,i)';
    caps_q=CAPS_Q(1:Num_Coeffs,i)';

    c1_I = c1*caps_i(1,1);  c1_Q = c1*caps_q(1,1);
    c2_I = c2*caps_i(1,2);  c2_Q = c2*caps_q(1,2);
    f1_I = f1*caps_i(1,3);  f1_Q = f1*caps_q(1,3);
    f2_I = f2*caps_i(1,4);  f2_Q = f2*caps_q(1,4);
    f3_I = f3*caps_i(1,5);  f3_Q = f3*caps_q(1,5);
    f4_I = f4*caps_i(1,6);  f4_Q = f4*caps_q(1,6);
    g1_I = g1*caps_i(1,7);  g1_Q = g1*caps_q(1,7);
    a2_I = a2*caps_i(1,8);  a2_Q = a2*caps_q(1,8);
    a3_I = a3*caps_i(1,9);  a3_Q = a3*caps_q(1,9);
    a4_I = a4*caps_i(1,10); a4_Q = a4*caps_q(1,10);
    b1_I = b1*caps_i(1,11); b1_Q = b1*caps_q(1,11);
    b2_I = b2*caps_i(1,12); b2_Q = b2*caps_q(1,12);
    b3_I = b3*caps_i(1,13); b3_Q = b3*caps_q(1,13);

    sim('adc4th_IQ_');
    Vpsd = (V);
    nfft    = Npts/2 ; %Number of FFT points
    window  = hanning(nfft) ;
    overlap = 1/2*nfft;
    signal = fin/fs * nfft + 1;
    cutoff = BW/fs * nfft + 1;
    [PSDw,f] = pwelch(Vpsd,window,overlap,'twosided',nfft,fs);
    PSD = PSDw * norm(window)^2 / sum(window)^2 * fs/2 ;
    SNR_cal
    SNR_OUTPUT(i) = 10*log10(SNR_inband);
    IRR(i)= -10*log10(PSD(signal)/PSD(nfft-signal+2));
end
save montecarlo_snr SNR_OUTPUT -append
save montecarlo_irr IRR -append
```

Fig. A.8 Code for Monte Carlo simulation of the Simulink Model

SIMULINK Model for SC Integrators with Finite Opamp DC Gains

The αβγ representation [1] can be used to model the impact of finite dc gain of the opamp on the transfer function of an ideal integrator. For an ideal delaying integrator the output $v_o(n)$ in discrete time domain can be expressed by:

$$v_o(n) = -kv_{in}(n-1) + v_o(n-1) \tag{A.1}$$

where k is the gain of the integrator. Due to the finite dc gain of the opamp, the modified non-ideal transfer function for a delaying integrator can be expressed as:

$$v_o(n) = -k\alpha v_{in}(n-1) + \beta v_o(n-1) + \gamma V_{OS} \tag{A.2}$$

The coefficient α modifies the gain of the non-ideal integrator, β shifts the pole of the integrator from the dc position, and γ is the suppression of the offset voltage V_{os} to the output of the integrator. With the help of αβγ representation, the transfer function of a delaying SC integrator can be written as:

$$\frac{v_o(z)}{v_{in}(z)} = \alpha k \frac{1}{z-\beta} + \gamma \frac{z}{z-\beta} V_{OS} \tag{A.3}$$

The (A.3) has been modelled in SIMULINK as shown in Fig. A.9 b. For the SC integrator shown in Fig. A.9 a the αβγ parameters are given in Table A.2:

The effect of the finite dc gain of the Opamp are included in the Simulink model of the SC integrators as shown in Fig. A.10.

Noise Analysis Using Mathematica

The noise transfer functions from each noise source to output of the modulator were determined in Mathematica. The integration of each power transfer function from dc to the signal-band edge represents the gain of the noise source to the output of the modulator. Fig. A.11 lists part of the code used to determine noise at the output of the modulator.

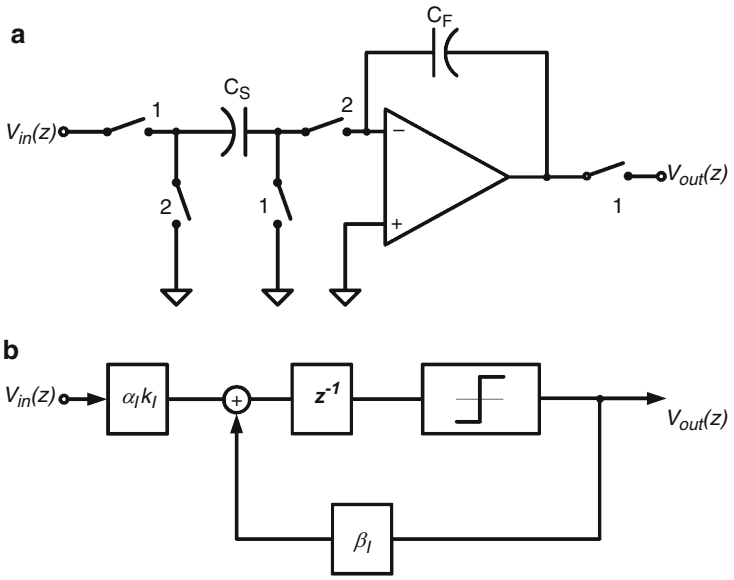


Fig. A.9 **(a)** Basic delaying SC integrator, **(b)** model of the delaying integrator used in SIMULINK

Table A.2 Expressions for the αβγ parameters for the delaying SC integrator shown in Fig. A.9 (a) for the integrator $|k| = C_S/C_F$, and $\mu \equiv 1/A_o$, where A_o is the opamp dc gain

α	$\frac{1}{1+(1+\lvert k\rvert)\mu}$
β	$\frac{1+\mu}{1+(1+\lvert k\rvert)\mu}$
γ	$\frac{\lvert k\rvert\mu}{1+(1+\lvert k\rvert)\mu}$

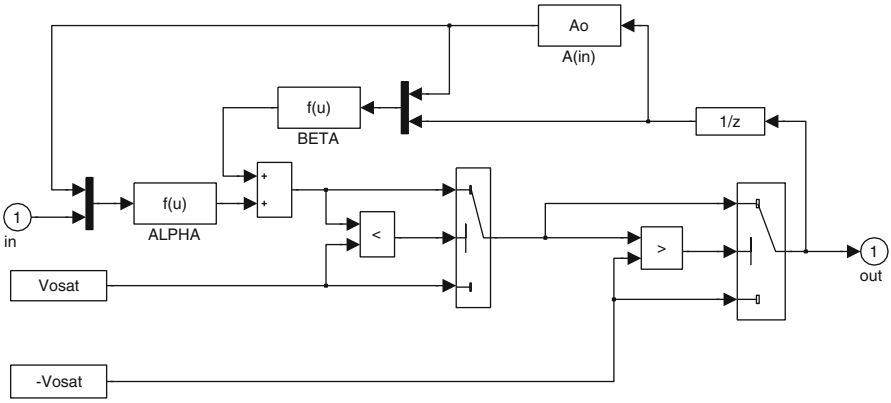


Fig. A.10 Model of the delaying integrator used in SIMULINK

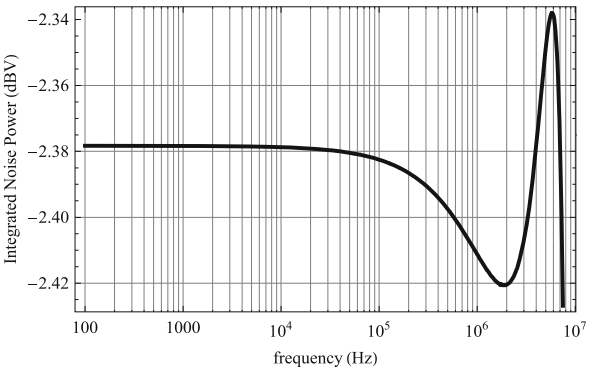
Noise due to C_1 and C_2

In[1960]:=

$$NTF_{i1} = \frac{C_1\ L_1}{1 + C_2\ L_1};$$

In[1961]:=
```
plot5 = LogLinearPlot[10 * Log[10, Abs[NTFi1]^2], {f, 100, fs / (1 OSR)},
  PlotStyle → {Black, Thick}, Frame → True, GridLines → Automatic,
  FrameLabel → {"frequency (Hz)", "Integrated Noise Power (dBV)"}]
```

Out[1961]=



In[1962]:=
```
NIntegrate[2 / fs (Abs[NTFi1])^2, {f, 0.0, fs / OSR}]
```

Out[1962]= 0.07211

In[1963]:=
$$RE\smile NTF_{i2} = \frac{Re[C_2]\ L_1}{1 + C_2\ L_1};$$
```
NIntegrate[2 / fs (Abs[RNTFi2])^2, {f, 0.0, fs / OSR}]
```

Out[1964]= 0.021163

In[1965]:=
$$IM\smile NTF_{i2} = \frac{Im[C_2]\ L_1}{1 + C_2\ L_1};$$
```
NIntegrate[2 / fs (Abs[INTFi2])^2, {f, 0.0, fs / OSR}]
```

Out[1966]= 0.103525

Fig. A.11 An example code for noise analysis of the model

Reference

1. W.-H. Ki, G.C. Temes, “Low-phase-error offset-compensated switched-capacitor integrator,” *Electronics Letters*, Volume 26, Issue 13,21 June 1990, pp. 957–959

Index